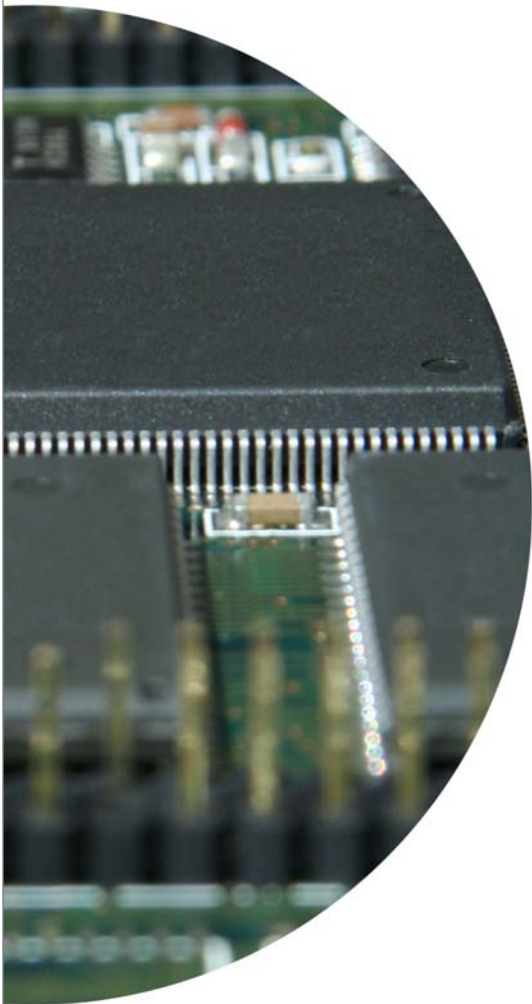


Silicon Solutions



Computer Systems, Inc.
MERCURY



FPGA Design Accelerators IP Cores Design Services

Minimizing Design Cycles for Maximum Profitability

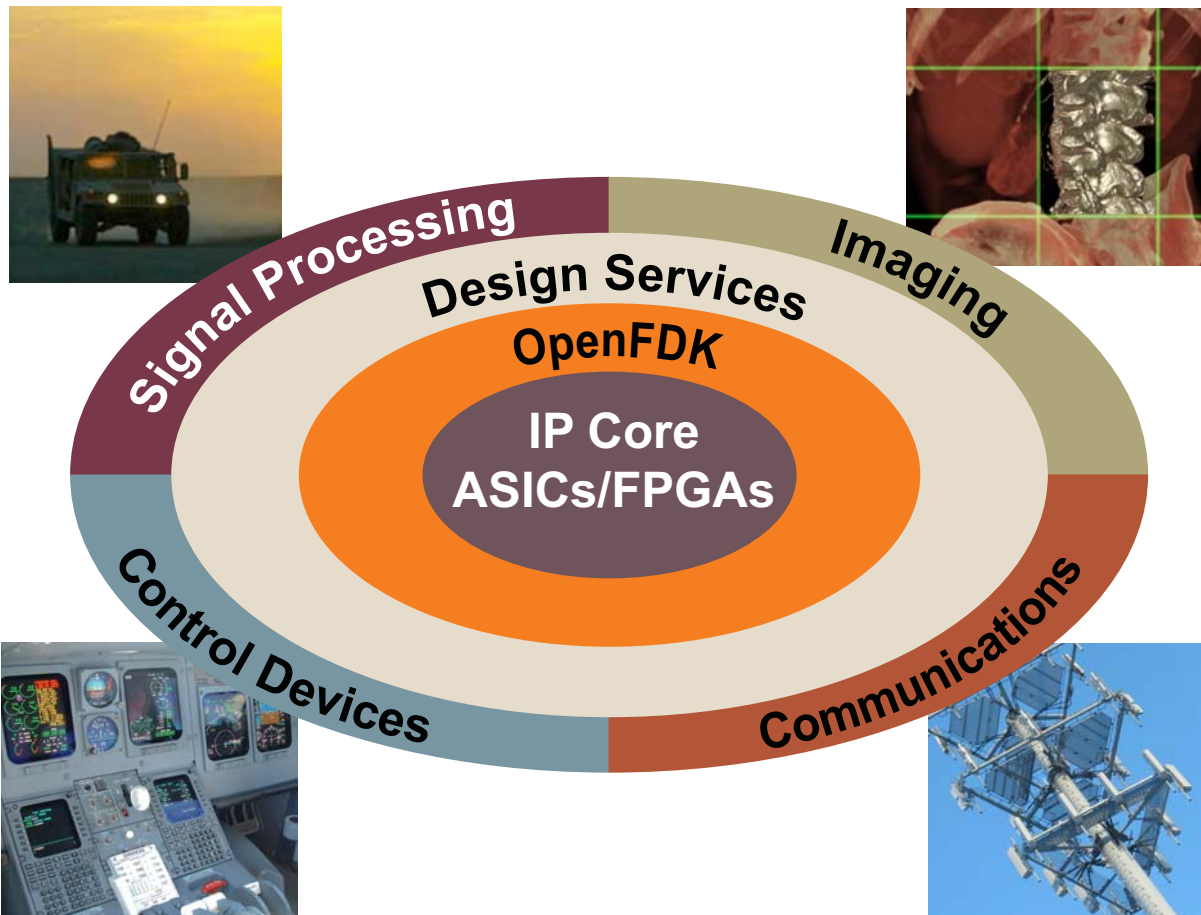
With the demand for higher complexity in integrated circuits (IC) ramping up for double-digit growth over the next decade, designers are looking for proven, reliable intellectual property (IP) to incorporate in their designs. New standards and more complex systems have placed added pressure on engineers, who are required to have expertise in many domains.

Once the systems have been designed, they must be validated and verified to ensure compliance to specifications and standards, which can consume as much or more time than the actual IP incorporation itself. Because overall profitability drops dramatically when products are delayed, IC designers are hard pressed to find the most efficient methods, tools, IP products, and services to minimize their design cycles.

Delivering Proven Technology

Mercury Computer Systems has over two decades of experience in the design and delivery of high-performance technology and systems for many industries, including aerospace and defense, life sciences, and telecommunications. Mercury pioneered switch fabric technology, including co-development with Motorola (now Freescale) of the RapidIO® interconnect IP.

Mercury is leveraging this expertise to offer robust IP cores, which have been developed after years of proven system implementation. Our high-performance verification IP can be used as a vendor-agnostic test aid, making it easier for designers to add new components and IP. For designs based on field-programmable gate arrays (FPGAs), our open standards-based FPGA Developer's Kit (OpenFDK) makes customizing and optimizing designs and algorithms faster with higher quality results and shorter development cycles.



Minimize Design Cycles with Mercury IP Cores, OpenFDK Tools, and Design Services

Accelerating FPGA Design and Integration

Current hardware trends indicate a movement away from fixed-purpose hardware. Field-programmable gate arrays (FPGAs) are rapidly emerging as the processor of choice for many of these processing-dense and space-constrained applications. Because FPGAs provide a higher level of flexibility for reconfiguration than other processor types, designers can use the same hardware for multiple functions. This increased need to integrate FPGAs into systems has made the development of new industry standards an imperative for software and IP to ensure interoperability of components at the module level.

Traditionally, FPGAs have been difficult to design and integrate into heterogeneous systems. However, Mercury has re-evaluated the design process to reduce costs through IP re-use, interoperability, and tools that enhance productivity. Our objective is to provide IP and tools that enable portability across platforms for a “design once, use many” mentality that reduces the effort involved in form-factor migration and technology upgrades. Mercury’s design methodology, which emphasizes simulation and verification, provides an environment that enhances the qualification of a design before moving to hardware, thereby reducing iterations of the tedious lab/debug cycle.

Open FPGA Developer’s Kit (OpenFDK) for Your System and Design Needs

The utilization of FPGA technology in systems covers a broad range: from an I/O device with standard protocols and pre-processing functions to a peer compute engine for application acceleration that needs direct memory access (DMA) functionality to provide the same look-and-feel as a general-purpose processor. The FPGA modules may be physically distributed or co-located in the same rack; the boards may be server blades or in a small 3U form factor for UAV deployment.

The full power of FPGAs is accessible through the Mercury OpenFDK, which contains software, intellectual property (IP) files, documentation, a validated default bitstream, and an intuitive API to help create and deliver FPGA solutions on a Mercury computing platform. Advanced features enhance the OpenFDK’s usability and accelerate product time to market.

Optimized for Embedded Design

The development of critical infrastructure IP components can become a tedious task for application designers, significantly increasing their design and validation time. To reduce engineering costs and speed up the design process, Mercury-supplied OpenFDK IP modules deliver a pre-validated environment and infrastructure for an application-ready platform. To ensure timing and performance, the IP modules are supplied as relationally placed macros (RPMs) that reside at the periphery of the FPGA

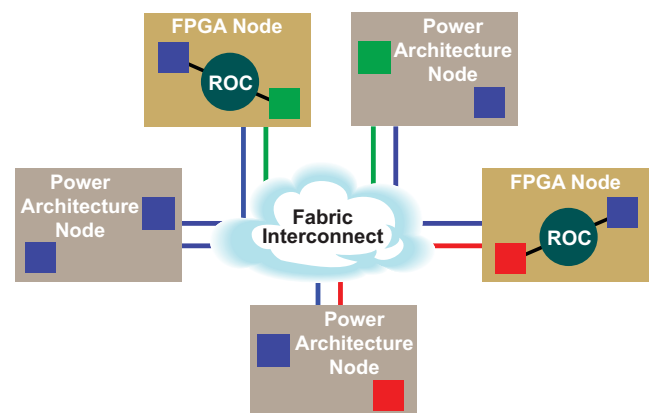
and allow application logic to interface with the communication infrastructure IP in a modular way to simplify placement and routing of the FPGA.

Standard Interfaces for Interoperability and Re-Use

The re-use of already developed and validated IP offers significant advantages, including the ability to port existing application code to different form factors with minimal modification and re-validation. To avoid the learning curve associated with many proprietary interfaces, Mercury’s OpenFDK IP is designed with standard Open Core Protocol™ (OCP) interfaces, which enable interoperability with IP components from other OCP-affiliated IP vendors. These OCP interfaces standardize the connectivity among components to provide the framework for modular FPGA IP design. Decoupling the interface from the underlying functional logic of a component permits the redesign of that function with minimal impact to the complete FPGA design. Isolation of the component through standard interfaces requires only that the component be unit-tested when the function is modified, instead of re-validating the entire system, facilitating the incorporation of last-minute application design changes into the system.

Accelerated System Integration

Complex systems require integration of FPGAs with other processors for maximum effectiveness. With our experience in heterogeneous computing and system architecture, Mercury has designed OpenFDK IP to include both IP modules and easy-to-use software API support for seamless communication between Power Architecture™ boards and FPGA boards. OpenFDK provides an extension of the fabric interconnect into the FPGA with the Mercury RoC (RACE®-on-Chip) bus. This multi-point, high-bandwidth communication pathway for the FPGA compute node enables system memory mapping and shared-memory buffer creation within the FPGA. The RoC architecture is responsible for the FCN’s dramatic high-speed data movement and seamless integration into the multicomputer switch fabric.

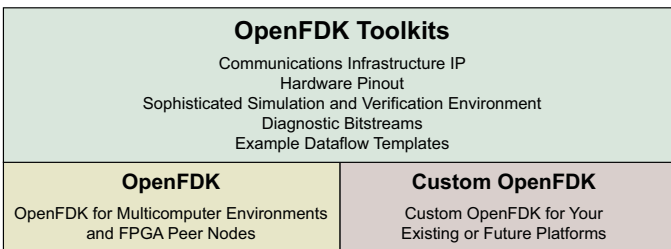


Design Reliability and Verification

Design verification can be an arduous and lengthy task for FPGA designers. Having the ability to fully verify the FPGA design through simulation can significantly reduce the cost and difficulties of lab verification. Mercury OpenFDK provides the necessary simulation framework to simplify FPGA design verification by providing a full set of bus functional models (BFMs) and simulation functions. The simulation environment delivers test cases that demonstrate the use of Mercury's library of functions to source/sink, monitor, and check data through interfaces provided as part of the communications infrastructure. Our verification environment delivers a complete system test environment that allows interactions through software simulators and transactors.

Customized OpenFDK to Fit Your System Architecture

Because of our experience in developing toolkits for a variety of FPGA devices and form factors, Mercury can efficiently develop a customized OpenFDK toolkit to fit your present and future

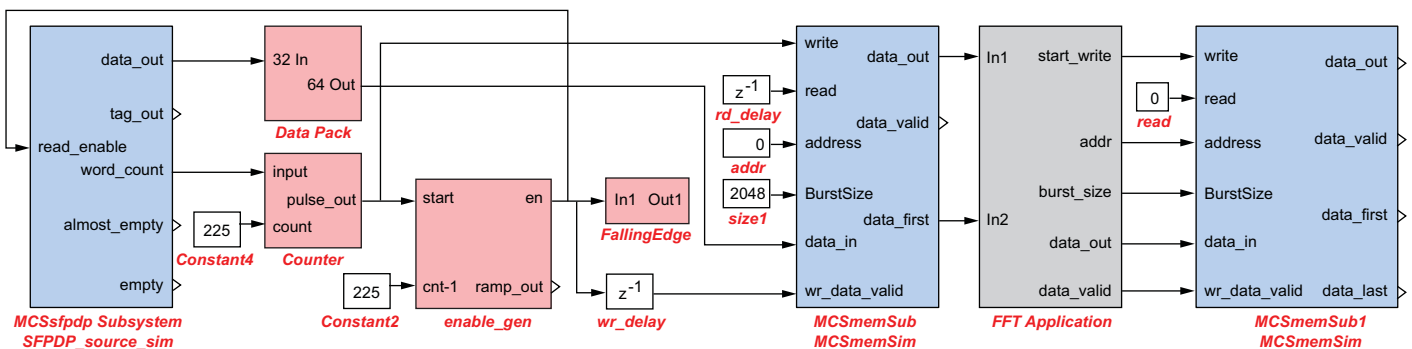


system architectures. As necessary, the communication infrastructure components and system verification suite are modified for the level of hardware abstraction. For boards that are not fabricated, our FPGA designers provide chip pin descriptions to ensure IP performance within the FPGA. Customized toolkits enhance productivity by allowing engineers to concentrate on system architecture and FPGA application design.

Ease of Use with Mercury Block IP Designer for Xilinx System Generator

The use of a consistent set of system-level tools results in reduced design risk and accelerated time to market. The MathWorks Simulink® product is a graphical user interface (GUI) based alternative to traditional HDL FPGA design methodology using blocksets. With the add-on blockset provided by System Generator® from Xilinx, this rich set of development tools gives you an easier way to design, test, and simulate high-performance digital signal processing systems from a system engineering level for FPGAs using pre-built, parameterizable functions and algorithms. In this environment, you can leverage Mercury OpenFDK IP along with your own IP in the form of Simulink models to develop your FPGA designs on a Mercury, proprietary, or custom platform.

Mercury Block IP Designer provides communications infrastructure IP blocks and their associated simulation models to be integrated in the System Generator environment. The clear separation between infrastructure and application IP blocks simplifies the porting of applications: merely replace the Mercury communications infrastructure blocks for a different platform.



System Generation Environment example

Proven, Reliable IP Cores and Silicon Solutions

Mercury's Expanding IP and Silicon Product Set



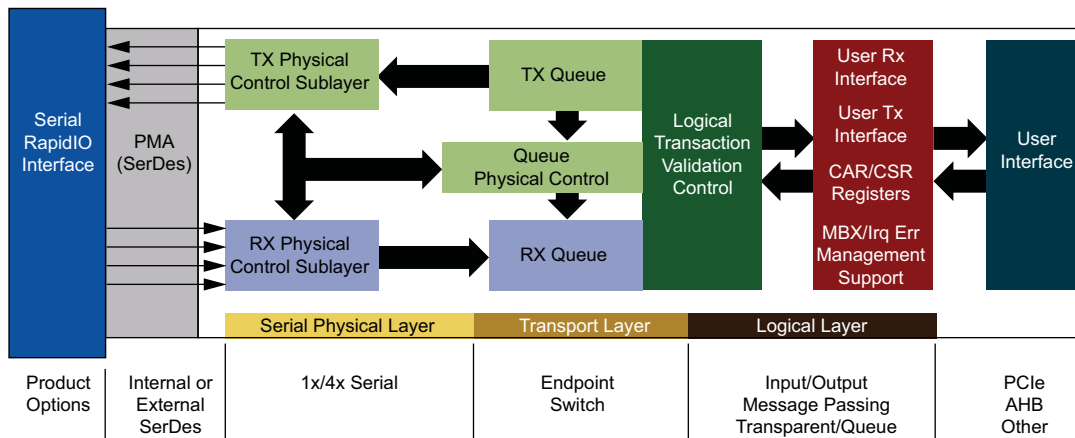
With knowledge and expertise acquired over 20 years, Mercury is leveraging our unparalleled experience with RapidIO technology to offer innovative serial RapidIO IP cores and silicon solutions for your most difficult design challenges.

Serial RapidIO IP Core

The Serial RapidIO IP Core is designed and architected to provide an end-to-end solution for a designer who needs to implement a RapidIO-based endpoint or switch. On one side, the core has a serial RapidIO interface. On the other side is a simple, implementation-neutral backside interface to ease the construction of add-on third-party bus interfaces.

The Serial RapidIO IP Core is ideal for use in a variety of communication applications, including reliable defense communica-

tions, base stations, edge routers, RNCs, enterprise switches, and other devices that require a high-speed interface. It can also be incorporated into high-end embedded compute and storage applications. The IP core is applicable for both FPGA and standard cell implementations. The IP core has been ported and supported in Xilinx®, Altera®, and Lattice® FPGA products. The serial RapidIO specification is currently supported for Revision Levels 1.2 and 1.3, with a migration path to support Revision 2.0.

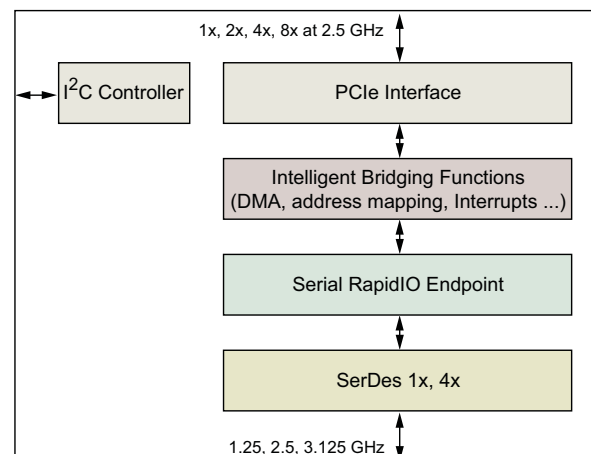


Serial RapidIO IP Core block diagram

RapidIO-to-PCIe Intelligent Bridge IP

The RapidIO-to-PCIe Intelligent Bridge IP block is architected to provide an end-to-end bridge solution between PCI Express® devices and RapidIO fabrics and devices. The core provides high-level functions such as multiple DMA engines, serial RapidIO mailbox message queuing and interrupts, address mapping, access protection, real-time event counters, and error management, among other functions. Concurrent I/O paths and sophisticated queuing with the intelligent bridge assure the highest utilization of available port bandwidth.

RapidIO and PCI Express are useful in a variety of communication applications, including base stations, edge routers, RNCs, enterprise switches, and other devices requiring a high-speed interface. PCIe chips have many I/O endpoints that can connect to a complex RapidIO fabric intelligently with the use of this bridge IP.

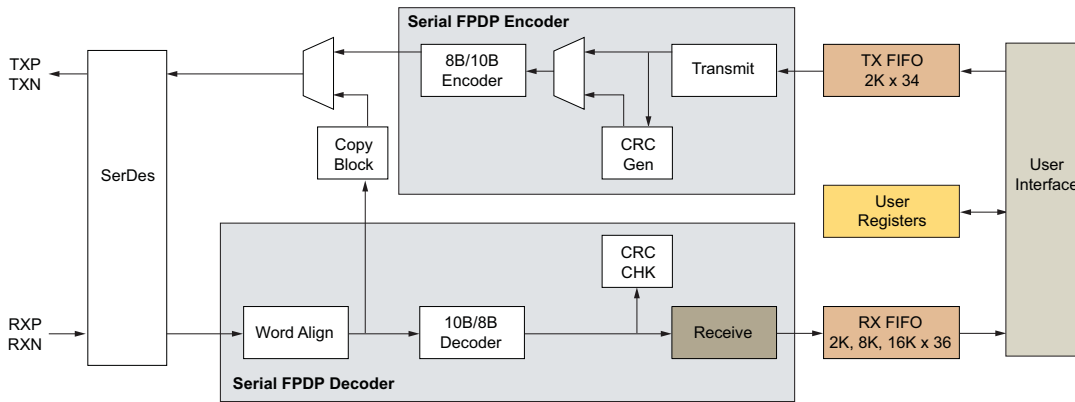


RapidIO-to-PCIe Intelligent Bridge IP block diagram

Serial FPDP IP

The Serial FPDP IP block is designed and architected to provide an end-to-end solution for a designer who needs to implement a communications data link. On one side, the core has a serial FPDP interface. On the other side is a simple FIFO backside interface to ease the construction of add-on third-party bus interfaces.

The Serial FPDP IP is ideal for use in a variety of front-panel communication applications, including sensors and data storage and retrieval applications.



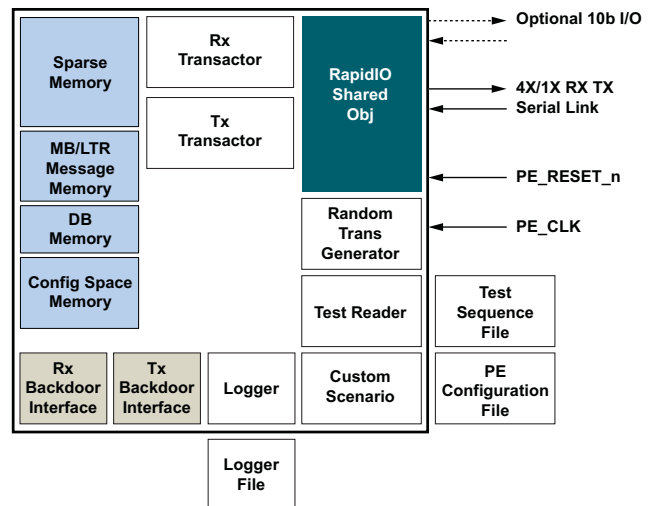
Serial FPDP IP block diagram

Serial RapidIO Verification IP

Serial RapidIO Verification IP allows developers to rapidly integrate RapidIO technology into their products for faster time to market. The Verification IP is highly configurable and comprehensive, and is designed to test the RapidIO interface at all layers, including logical, transport, and physical. It addresses the needs of a variety of solutions, including endpoint, bridge, and switching applications.

This verification IP automatically creates a significant amount of the required serial RapidIO transactions and checks the responses. It performs functional and compliance checklist coverage to monitor progress against goals. By providing support for constrained random testing, it enables faster debugging of proprietary functionality, corner case testing, and error checking.

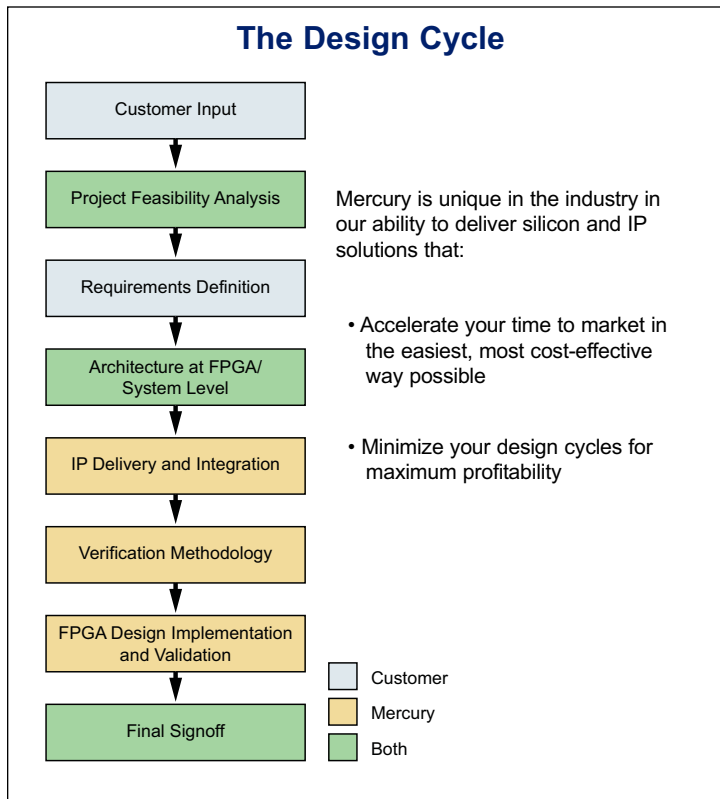
The Verification IP is highly configurable and architected with enhanced functions to provide an end-to-end solution for designers who need to implement a serial RapidIO-based application in either ASICs or FPGAs.



Serial RapidIO Verification IP processing element block diagram

Mercury Is Committed to Your Success

Mercury's team of talented service professionals offers comprehensive FPGA application design services and FPGA system integration, leveraging our years of experience in digital signal processing technology. Whether you are looking for a total turnkey solution or a solid IP foundation to develop your algorithm, Mercury's technology experts can design an innovative solution for you.



Our Customers Define Success

The Challenge

A leading communications company asked Mercury's engineering team for help on an interesting challenge: reduce their development time by providing the proficiency to incorporate FPGAs in their system architecture, while allowing their software and hardware teams to work in parallel during the development efforts.

The Mercury Advantage

Mercury worked closely with the customer to define an architecture that would be conducive to parallel operation and be distributed in FPGAs. Mercury provided an FDK Streaming IP that assisted both the software and hardware teams to develop code within the infrastructure. The FDK streaming IP provided the high-speed interconnect between onboard FPGAs at 6.4 Gbps links and off-board at 3.125 Gbps, enabling real-time system performance throughout the development.

The Results

With the assistance of the Mercury engineering team, a complex system of nine FPGAs was developed ahead of schedule by deploying hardware and software resources simultaneously. Using the FDK streaming IP product helped the customer reduce development time by 60%.

For more information on Mercury's silicon and IP products and design services, contact your Mercury sales representative or call 866-627-6951.

Mercury Computer Systems, Inc. – Where Challenges Drive Innovation

Mercury Computer Systems (www.mc.com) is the leading provider of computing systems and software for data-intensive applications that include image processing, signal processing, and visualization. We work closely with customers to architect comprehensive, purpose-built solutions that capture, process, and present data that have a meaningful impact on everyday life – from detecting aneurysms, designing safer, more fuel-efficient aircraft, identifying security threats, and discovering oil; to developing new drugs, and visualizing virtually every aspect of scientific investigation.

Mercury is based in Chelmsford, Massachusetts and serves customers worldwide through a broad network of direct sales offices, subsidiaries, and distributors. We are listed on the Nasdaq National Market (NASDAQ: MRCY). Visit Mercury at www.mc.com.

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