

Serial RapidIO IP Core

Industry-Standard, High-Performance, Packet-Based Interconnect Technology

- Provides both RapidIO endpoint and switch applications
- Simplifies the construction of add-on third-party bus interfaces
- Ideal for use in a variety of high-end embedded compute applications
- Implements an advanced buffer management scheme
- Targets both FPGA and standard cell technologies



The RapidIO® Interconnect Architecture is an industry-standard, high-performance, packet-based interconnect technology that provides a high-speed interconnect between NPUs, CPUs, and DSPs. It addresses the need for a standards-based, high-speed, reliable interconnect and is targeted at the networking, embedded, and storage markets. Serial RapidIO allows chip-to-chip, board-to-board, and system-to-system communications scaling to 10 Gbps and beyond.

Mercury Computer Systems' Serial RapidIO IP Core is designed for the growing RapidIO market. The core is a high-performance solution that is independent of physical layer designs, implementation tools, and target technology. It is capable of addressing a variety of solutions, including endpoint and switching applications.

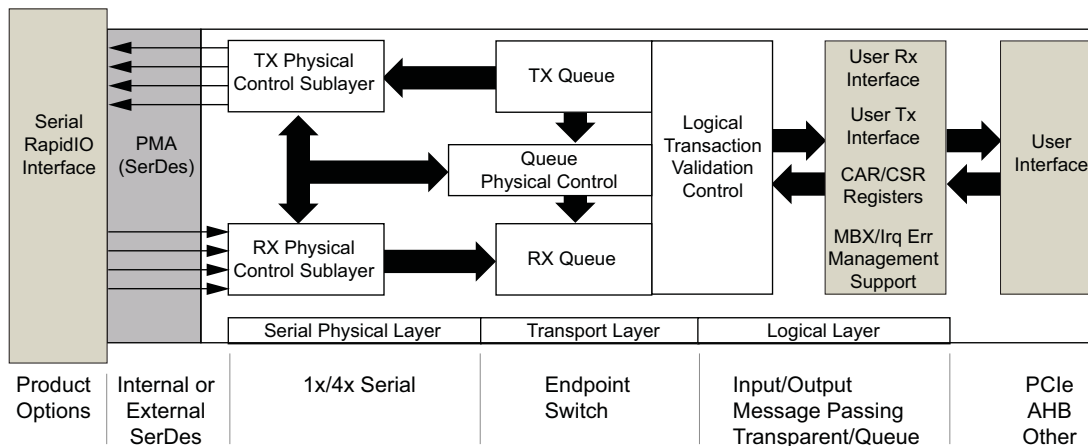
As the pioneer of heterogeneous switch fabric-based computing and co-developer of the RapidIO technology, Mercury is uniquely equipped with the system and application expertise, and the support and consulting resources focused on RapidIO. No other supplier of RapidIO IP can provide a proven product with such high performance and flexibility, as well as the long-term system-level testing that Mercury has already conducted on its IP cores.

High-Performance, High-Function Core

Mercury's Serial RapidIO IP provides a range of solutions for use in a variety of applications. It is architected to provide an end-to-end solution for designers who need to implement a serial RapidIO-based endpoint solution in either ASICs or FPGAs, and it can be designed into multi-port switches. The core provides a serial RapidIO interface on one side and a simple implementation-neutral user interface on the other to ease the construction of add-on third-party bus interfaces.

The serial RapidIO IP solution is a complete high-performance, high-function core. It incorporates a logical layer, a transport layer, and a physical layer, and supports input/output and message-passing logical layer standards.

RapidIO is ideal for use in a variety of communication applications including base stations, edge routers, RNCs, enterprise switches, and other devices requiring a high-speed interface. It can also be incorporated into high-end embedded compute applications.



Specifications

Language	Verilog HDL
Synthesis	Synopsys®/Synplicity®
Technology	0.13 µm or better and FPGA
Simulation	Model Technology
Support for:	Serial specification 1.2 GHz, 2.5 GHz, 3.125 GHz 1x and 4x serial interfaces Error management extensions 34-bit addressing All legal data payload sizes up to 256 bytes Input/output and message-passing protocols Receiver-controlled and transmitter-based flow control All transaction flows and priorities Multicast event support
Availability and Serviceability	Available now
Product Options	Single or multi-use license Soft IP core: RTL source code, synthesis scripts, etc. Comprehensive documentation package
Compliance	RapidIO specification, Revision 1.2

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