

Technology Overview: VITA 41 (VXS)

INTRODUCTION

This Mercury Technology Overview is one in a series designed to provide a deeper look at the array of Mercury technologies available to designers of high-performance signal processing systems.

In this overview, we look at VITA 41 (VXS), a computing standard that introduces serial switch fabric technology into the VME64 architecture. We discuss the motivation behind creating a new standard, the primary issues that its architects were trying to solve, and some points in the architecture that may help you make decisions when implementing systems using the standard.

To get the most from this overview, you should already be familiar with these resources:

- Mercury Technology Brief: Evolution of Computing Standards for Signal Processing
- Any of several computing standards based on the popular Eurocard format, such as VME64 or CompactPCI®

This overview does not represent the complete technical detail available in the specifications discussed, but it does draw on information from those specifications. Copies of complete specifications are available for purchase upon release as ANSI standards from VITA, the trade association responsible for their development, at www.vita.com.

CREATING VXS

VMEbus continues to be the technology of choice for systems requiring high-performance, longer life cycles, durability, and a highly flexible combination of features from which systems designers can choose.

VME Switched Serial, or VXS, introduces new features into the existing VMEbus technology base, further extending the life-cycle of existing board products while simultaneously offering distinct improvements to the architecture for new system designs.

VXS is an evolutionary change for VME users. It adds high-speed serial fabric technology in a fashion that does not require revolutionary change in system architecture. In short, VXS remains backward compatible with previous generations of VMEbus.

There are three primary motivations behind the creation of VXS: improved bandwidth, backward compatibility to VME64, and increased power delivery.

Improved bandwidth – Using a choice of modern serial switch fabric interconnects, along with the latest VME 2eSST protocols for parallel bus transfers, system designers have access to dramatically improved bandwidth. Compared to VMEbus bandwidths in the 40 MB to 60 MB range, VXS systems can achieve over 45 Gigabytes per second (GB/s) using today's fabric speeds and switch technology, and should grow to 180 GB/s as fabric speeds and switch technology improves.

Backward compatibility to VME64 – By preserving the electrical and mechanical properties and locations of the VME64 P1 and P2 connectors, and ensuring that the new P0 connector does not interfere with non-P0 cards, standard VME64 backplane slots are created in VXS systems and insertion and use of legacy VMEbus cards is possible. Hybrid backplanes are also allowed in VXS systems, so even VME64 boards with original P0 connectors can be accommodated.

Increased power delivery – Designers using today's class of powerful processors are finding the VME64 specification of 35W power inflow limiting. Using more sophisticated analysis techniques, the 5-row DIN 41612 connectors specified in VME64x are more capable than the original VME64 specification of 1A per power pin. VXS references ANSI/VITA 1.7, which studied the capability of these DIN connectors in depth and found them capable of supplying nearly twice the +5V power as earlier thought.

OVERVIEW OF VXS

VXS is based on the VITA 41 family of specifications. Architects created VXS as a series of layered or “dot” specifications. The base specification describes common elements, while extension specifications define the use of specific serial fabrics, live insertion, system management and other topics as needed. Current VITA 41 specifications include:

- VITA 41.0 VXS
- VITA 41.1 InfiniBand® Protocol on VXS
- VITA 41.2 Serial RapidIO® Protocol on VXS
- VITA 41.3 VXS Ethernet 1000 Mb/s Baseband IEEE 802.3 Protocol Layer Standard
- VITA 41.4 VXS 4X PCI Express® Protocol Layer Standard
- VITA 41.10 Live Insertion System Requirements for VITA 41 Boards
- VITA 41.11 VXS Rear Transition Module Standard

Payload and Switch Cards

The VXS base specification describes two types of cards – payload and switch – and a corresponding backplane slot for each. It also describes how backplanes can be designed for various configurations, such as star, dual-star, and daisy-chain, although it does not mandate a topology. The base specification provides a common set of definitions on which dot specifications for implementation of specific serial switch fabric technology can be overlaid.

A VXS payload card follows the basic construct of a 6U VME64 card with an added high-density, high-speed P0 connector and corresponding alignment and keying features. Each payload board supports up to two serial ports. If a payload board implements only one port, it is Port A. The specific link configurations are determined in the appropriate dot specification.

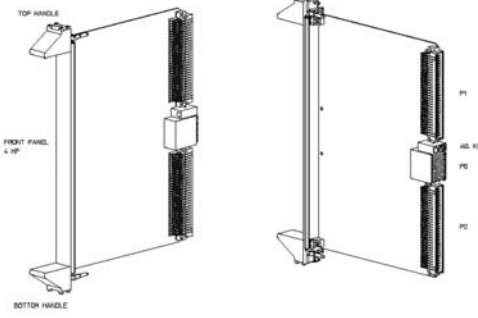


Figure 1. VX S Payload Card

A VX S switch card, a new design, is architected to provide an aggregation point for serial fabric connections, and uses multiple high-speed differential signaling connectors to provide the necessary high-speed pins. Switch cards also have an enhanced power connector and a user-defined I/O connector. To accommodate the increased insertion and removal forces, switch cards use a larger front-panel handle providing increased leverage.

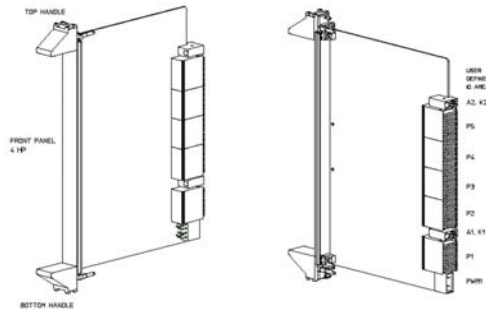


Figure 2. VX S Switch Card

VX S also provides alignment and keying instructions for payload and switch slots. Payload cards have one alignment and keying device, while switch cards have two. Keying values are defined in each protocol layer dot specification.

MultiGig RT Connector

With increased interconnect speeds, higher pin density, reasonable insertion forces, and environmental characteristics as design goals, Tyco undertook development of a new connector family in 2001. Finally dubbed the MultiGig RT family, this new connector is the solution for VX S.

One unique feature of this connector is the wafer design, where contacts and internal routing are formed using miniature printed circuit cards. This design implements several key objectives, described in the following sections.

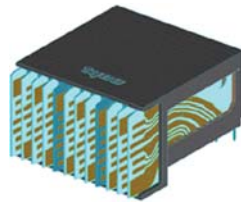


Figure 3. Tyco MultiGig RT Connector

Signal Integrity

Chiclet wafers are available in several formats suited for power, single-ended signaling, or differential signaling. Each differential contact pair is currently rated at signal speeds of up to 6.25 Gigabits per second (Gb/s) using today’s driver silicon. This rating is expected to evolve to over 10 Gb/s as technology continues to improve.

To affirm integrity, eye pattern testing was performed on a physical backplane, with acceptable signal performance found at the rated speeds. Specific test conditions documented by VITA were: 16” FR4 backplane traces, 4” FR4 daughtercard traces, top layer via connection, no counterboring, 27-1 pseudo-random bit string. Observed results under these conditions were a 46.8% eye opening.

Insertion Force

A goal of the VX S design was to create cards that could be inserted and removed using reasonable manual forces generated by the front-panel handles. For the VX S payload card, these are the IEEE 1101.10 handles as found in the VME64 specifications. For the VX S switch card, there are new handles designed to provide a greater lever arm for the additional high-density connectors.

VITA held a mechanical compatibility workshop for VX S prototypes from various vendors during 2004. During the workshop, measurements were made on insertion and removal forces for payload and switch cards. These forces were deemed reasonable for manual efforts.

Table 1. VX S Payload Card Forces

Payload Board	Mating Force		Unmating Force	
	Test Value	Maximum	Test Value	Minimum
P0	77N	101 N	37 N	20.3 N
<i>N = Newtons</i>				

Table 2. VX S Switch Card Forces

Switch Board	Mating Force		Unmating Force	
	Test Value	Maximum	Test Value	Minimum
P5	82 N	108 N	39 N	22 N
P4	82 N	108 N	39 N	22 N
P3	82 N	108 N	39 N	22 N
P2	82 N	108 N	39 N	22 N
P1	82 N	108 N	39 N	22 N
PPWR1	22 N	22 N	22 N	22 N
SUM	463 N (105 lbf)	586 N (105 lbf)	215 N (105 lbf)	136 N (105 lbf)

Environmental Factors

Durability is a key consideration for system architects looking to use VXS, and the designers of the specification considered this factor in the selection of the MultiGig RT connectors.

MultiGig RT connectors are designed for 250 insertion cycles and have been extensively tested in environments according to MIL-STD-1344A, including vibration and shock, thermal shock, humidity, salt fog, dielectric withstanding voltage, low-signal level contact resistance, and insulation resistance. These tests were performed by Tyco and augmented by further testing from VXS Working Group members and the U. S. Navy. The conclusions indicated that the MultiGig RT family is a robust connector system capable of withstanding the harsh environments found in military/aerospace environments.

VXS BACKPLANE

Star – In a star configuration, each payload card connects to a single switch card. Star configurations require a switch card, scale up to 18 cards, and have no redundant fabrics.

Dual Star – In a dual-star configuration, each payload card connects to two separate switch cards (which can be interconnected) for higher reliability and/or load balancing. Dual-star configurations require two switch cards for fabric redundancy and scale up to 18 cards. The specification discusses an example of a dual-star topology.

Mesh – In a mesh configuration, each card is directly connected to every other card. With the two available ports, up to three payload cards can be interconnected without using a switch card.

Daisy-Chain – In a daisy-chain configuration, each card is directly connected to its nearest neighbors. When a packet travels from one end of the chassis to another, it passes through each board. Daisy-chain configurations do not require a switch card but have two main trade-offs. First, the bandwidth between two neighboring boards is shared with all the other boards in the system that want to communicate through that part of the daisy-chain ring. Second, daisy-chain topologies are considered less reliable, because a failure in any card would bisect the backplane.

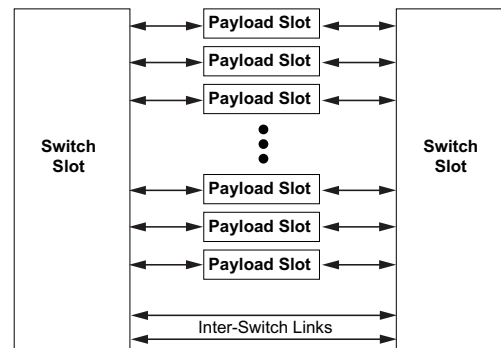


Figure 4. Dual-Star Topology

VME64 and VME2eSST continue to form a useful path for control and low-rate data traffic in a VXS system. While fabrics such as RapidIO certainly could handle control traffic, there are architectural advantages in latency and simplicity gained by keeping high-rate data transactions on a separate physical interconnect from control and low-rate data transactions. Simpler forms of I/O that have been designed for VME64 with low data rates can continue to be used without redesign.

VXS POWER

ANSI/VITA 1.7-2003, Increased Current Level for 96 Pin & 160 Pin DIN/IEC Connector Standard, describes an improvement to the power delivery capability of the DIN 41612 connector used for VME64 J1 and J2. When these connectors were originally designed, they were rated for a current capacity of 1A per pin. In the VME64 definition, this offered a power intake to a slot of 35W from the primary +5V supply. This level of power was sufficient for many years, but with the advent of today's powerful microprocessors, Field-Programmable Gate Arrays (FPGAs), and digital signal processors (DSPs), it has become limiting.

Under ANSI/VITA 1.7, analysis of the current 5-row VME connector was undertaken to better determine its exact capabilities, including such variables as pin locations and heat rise. The conclusion of this analysis was that the basic connector design and pinout defined in VME64 is capable of 2A per power pin. This offers VXS board designers relief from the 35W prior limit, with practical applications now in the 50W to 60W range.

VME64 COMPATIBILITY WITH VXS

Backward compatibility is likely to be important to users looking to migrate forward from VME64 into VXS systems. Payload slots are fully compatible with existing VME64 cards that do not contain a P0 connector. For a pre-VXS VME64 card installed into a VXS slot, the VME64 connectors P1 and P2 on the payload card simply mate into the backplane normally, and the backplane J0 does not interfere or make contact with the card. Also, system designers can consider using hybrid backplanes that create VME64-only slots by omitting P0.

CONDUCTION COOLING

Many VMEbus applications require conduction cooling. The VXS Working Group has a study underway to investigate a profile of the standard suitable for conduction cooling. One key issue that needs to be addressed is clearances around the high-speed connectors on the switch card to allow for the required conduction rails to pass up the edges of the card. For applications requiring conduction cooling, the VPX and REDI standards should be investigated as well.

VXS COOLING

While VXS offers increased power inlet capability, it makes no changes to cooling and offers no increased thermal removal methods beyond the conventional VME64 slot configuration. VXS slots maintain the same 0.8" pitch as with VME64, and are designed for cooling via forced-air convection methods.

MAPPING FOR SERIAL RAPIDIO

Perhaps the key motivation behind VXS was the introduction of high-speed serial switch fabrics into the architecture. A dot specification, Serial RapidIO Protocol Layer for VXS, extends the architecture and defines use of serial RapidIO as the backplane fabric. Guidelines for the use of serial RapidIO as in-band management and Inter-Integrated Circuit (I2C) as out-of-band management are also described. Mercury teams led the definition of the VXS mapping for serial RapidIO.

In VXS, each payload card supports up to two 4x LP-serial RapidIO links with differential signaling pairs mapped onto P0. These links have been mapped with enough ground pins included to support the high-speed signaling required by serial RapidIO.

Table 3. VXS Payload Card P0 Mapping for Serial RapidIO

	Rows L/K	Rows J/I	Rows H/G	Rows F/E	Rows D/C	Rows B/A
1	GND	RFU/PA RR1	GND	PA TX0 -/+	GND	PA RX0 -/+
2	RFU/PA RR2	GND	PA TX1 -/+	GND	PA RX1 -/+	GND
3	GND	RFU/PA SCL	GND	PA TX2 -/+	GND	PA RX2 -/+
4	RFU/PA SDA	GND	PA TX3 -/+	GND	PA RX3 -/+	GND
5	GND	RFU	GND	RFU	GND	RFU
6	RFU	GND	RFU	GND	RFU	GND
7	GND	RFU	GND	RFU	GND	RFU
8	RFU	GND	RFU	GND	RFU	GND
9	GND	RFU	GND	RFU	GND	RFU
10	RFU	GND	RFU	GND	RFU	GND
11	GND	RFU	GND	RFU	GND	RFU
12	RFU/PB RR1	GND	PB TX0 -/+	GND	PB RX0 -/+	GND
13	GND	RFU/PB RR2	GND	PB TX1 -/+	GND	PB RX1 -/+
14	RFU/PA SCL	GND	PB TX2 -/+	GND	PB RX2 -/+	GND
15	GND	PEN*/PB SDA	GND	PB TX3 -/+	GND	PB RX3 -/+

Notes:

- PA = Port A, PB = Port B
- TX = transmit, RX = receive (with respect to the payload card).
- Signal pairs 0-3 on each port correspond to serial RapidIO signal pairs 0-3.
- If a payload card implements only one port, it is Port A.
- PA_SCL and PA_SDA are defined as an I2C-compatible serial link. PA_RR1 and PA_RR2 are reserved signals associated with serial link A.
- PB_SCL and PB_SDA are defined as an I2C-compatible serial link. PB_RR1 and PB_RR2 are reserved signals associated with serial link B.
- Signal PEN* is power enable, defined in the VITA 41.10 Live Insertion standard.
- RFU pins are reserved for future use.

Also in VXS, switch cards are defined supporting up to eighteen 4x serial RapidIO links for communication with payload cards and additional 4x serial RapidIO links for communications with other switch cards, again with links comprised of differential signaling pairs mapped on to connectors P2-P5.

The RapidIO serial physical layer interface offers a XAUI (10G Attachment Unit Interface) compatible electrical interface operating at 1.25, 2.5, or 3.125 Gb/s (with an effective data rate of 2.5 Gb/s after 8b/10b encoding). Because it is XAUI compatible, RapidIO technology is aligned with embedded backplane needs and can leverage the volume ecosystem around the XAUI physical layer. The specification defines one- and four-lane versions to offer bidirectional bandwidth between 2 Gb/s to 20 Gb/s per link. Four lanes provide a 10 Gb/s port, full duplex. In addition, the serial RapidIO interface can scale incrementally from 1 Gb/s up to 10 Gb/s, offering more flexibility for the designer.

To software, the RapidIO interconnect looks like a traditional microprocessor or peripheral bus, so hardware implementations can hide functions such as discovery and error management from software, unless a software system elects to participate. This is another example of the RapidIO technology's inherent compatibility with legacy system and application software. RapidIO presents a smooth migration path from RACE++[®] for users of Mercury systems, as applications using the Parallel Acceleration System/Data Reorganization Interface (PAS[™]/DRI), Message Passing Interface (MPI), or other middleware libraries can be recompiled with minimal software changes.

VXS concentrates on the definition of inter-board connections, but one advantage of serial RapidIO is as an intra-board connection. Many of today's advanced processors, such as the Freescale[™] MPC8641 dual-core PowerPC processor or the Texas Instruments TMS320C6455 DSP offer on-chip serial RapidIO ports with direct connection into the processor. By extending the connections from processors throughout the system via the inter-board backplane and switch card connections, systems can scale their processing power very effectively without unnecessary bridging between interconnect schemes.

Mercury is a leader in RapidIO, which presents a natural migration path for RACEway users. For a complete discussion of RapidIO technology, visit www.rapidio.org and look in the Education section for the Technology Overview and Applications presentation along with other information.

While RACE++ offers a 267 MB/s transfer rate per port, RapidIO (2.5 GB/s) can dramatically increase system bandwidth through use of simultaneous transactions via multiple ports in a switched system architecture such as dual-star or mesh.

REAR TRANSITION MODULES

VXS anticipates the use of rear system I/O presented through the backplane instead of from the front of a module. Rear transition modules (RTMs) are a way to provide industry-standard connectors for onboard resources as a board designer confronts the limited amount of space on the front panel of a VME card. RTMs also permit an improved cabling configuration by allowing some or all of the cabling from a board to be routed out the rear of a chassis, thus providing unobstructed access to the faceplate. RTMs are defined in VXS in a dot specification.

VXS IN DEVELOPMENT AND USE

Mercury engineering teams are deeply involved in the definition of VXS, leading development of the specification. Many other organizations also support the efforts, including several leading embedded computing manufacturers and several major defense electronics system integration companies. This combination of architects from leading equipment vendors, integrators, and users is helping to make the standard better at meeting interoperability goals.

Vendors including Mercury began introducing VXS-compliant products in 2005. A key element of the VXS architecture is the ability to use VME64-compliant cards in a VXS system, further increasing the choices of payload cards for consideration. With fabric moving from RACE++ over P2 to serial RapidIO over P0, there is a big win in terms of freeing P2 for user-defined purposes.

Along with Mercury Computer Systems, representatives from the following organizations are participating in the working group efforts of the VXS standards development process:

Amphenol Backplane Systems
The Boeing Company
Critia Computer, Inc.
Curtiss-Wright Controls Embedded Computing
Elma Bustronic Corporation
FCI Electronics
Foxconn Electronics Inc.
GE Fanuc
General Dynamics Advanced Information Systems
GHz Systems, Inc.
Hybricon Corporation
IBSi
Motorola Embedded Communications Computing
Northrop Grumman Electronic Systems
Parker Hannifin
Pentair/Schroff
Radstone Embedded Computing
SBS Technologies, Inc.
Spectrum Signal Processing, Inc.
Tyco Electronics
U.S. Navy - Naval Surface Warfare Center, Crane Division (NSWC Crane)

CONCLUSION

VXS is a standard that combines parallel VMEbus with enhancements to support serial switch fabrics, including serial RapidIO and others over a high-speed P0 connector. Backward compatibility to VME64 systems is maintained with existing backplanes that do not have a conflicting P0 scheme. Combining the VME2eSST parallel bus with switch fabric technologies such as serial RapidIO for multi-point, high-speed data transfers creates excellent choices for embedded designs.

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