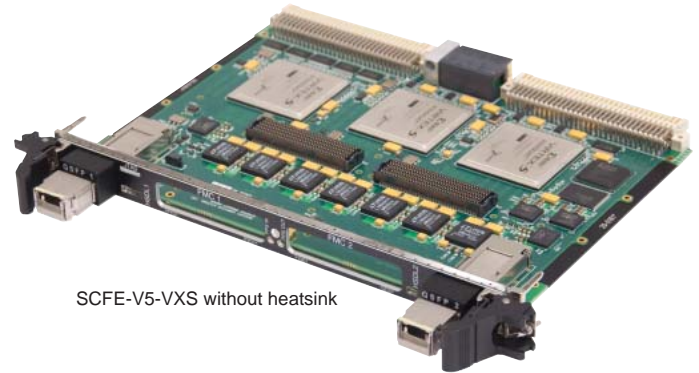


Echotek Series SCFE-V5-VXS Virtex-5 Based FPGA Processing Engine

High-Performance FPGA Processing

- Ultimate processing power with three Xilinx® Virtex™-5 SX240Ts or LX330Ts
- High-speed fiber connectivity via the front panel
- Optional VITA 57 FMC sites for flexible I/O enhancements
- High-speed VXS interface or RACE++® interface



SCFE-V5-VXS without heatsink

The Echotek® Series SCFE-V5-VXS Virtex™-5 Based FPGA Processing Engine from Mercury Computer Systems provides high-performance processing for applications requiring extreme FPGA processing power. Utilizing the largest FPGAs available from market-leader Xilinx®, the SCFE-V5-VXS solves the toughest computing problems in a cost-effective form factor. The other interfaces on the card, including the QSFP fiber transceivers and the VITA 57 FMC mezzanine sites, combine with the FPGAs to create an interoperable, upgradeable solution for a vast number of platform configurations.

FPGA Processing Power

The SCFE-V5-VXS implements three Xilinx Virtex-5 SX240T or LX330T FPGAs. These 1738 pin-package FPGAs offer the ultimate in processing power, supplying the user with up to 3168 raw DSP48e slices. Each FPGA is connected via a network of HSDL links and high-speed GTP lanes, allowing maximum flexibility when implementing complex designs. Two FPGAs function as prosecutors, the first to receive and process data from either the QSFPs or the FMC sites. The third FPGA acts as the governor, interfacing with the backplane by implementing either the high-speed VXS or a RACE++® interface.

All the Virtex-5 FPGAs are initially populated with standard IP loads that include firmware cores from Mercury's enhanced EchoCore™ library. They are also user-programmable for implementing customer-specific application features.

FPGA Connectivity

The SCFE-V5-VXS FPGA connectivity consists of a network of HSDL links and GTP serial lanes between the FPGAs and various interfaces, allowing for maximum flexibility when moving data. Each of the two prosecutor FPGAs is connected to its respective FMC site via 80 LVDS pairs and 10 GTP serial lanes. An additional four GTP serial lanes connect them to their QSFP interface. The two prosecutor FPGAs can share data via 32 full-duplex HSDL links and also with the governor FPGA via a 16-lane full-duplex HSDL interface, an 8-lane full-duplex HSDL interface, and 8 GTP serial lanes.

EchoCore™ Advantage

Mercury's EchoCore firmware streamlines the development of FPGA-based applications. These cores are optimized to maximum performance for a range of common operations. They are designed with straight-forward interfaces for application-specific algorithm IP, greatly reducing the time required to create complete solutions.

FMC Sites

The SCFE-V5-VXS can be configured with two FMC (VITA 57) mezzanine connectors, expanding the board's ability to support a variety of I/O interfaces. Designated as the SCFE-V5-FLX-VXS, this version of the module connects each prosecutor FPGA to an FMC site via 80 LVDS pairs and 10 GTP links, providing flexible I/O paths to and from the board.

Fiber Connectivity

The card has two quad small-form-factor pluggable (QSFP) fiber interfaces. They each provide four fiber lanes to a processor FPGA, running at up to 3.125 Gb/s per lane (maximum theoretical) for high-speed data communications. These fiber interfaces are highly effective when inter-chassis communication is required.

Memory

The SCFE-V5-VXS features two types of memory in support of each Virtex-5 FPGA, enabling their use in multiple deployment applications. DDR2-SDRAM is provided in a 256-MB bank and utilizes a 300-MHz, 32-bit link to its respective FPGA for a total theoretical memory bandwidth of 2.5 GB/s, half-duplex. The faster QDR2-SRAM is provided in a 9-MB bank and is designed with a 200-MHz, 32-bit bus for a total theoretical bandwidth of 1.6 GB/s, full-duplex.

SecureConfig

SecureConfig is Mercury's latest enhancement for FPGA configuration. Using the SecureConfig approach, not only does the SCFE-V5-VXS allow easy FPGA configuration, but it also allows classified images to be used without compromising security. The user is given the option to load FPGA images to either non-volatile or volatile memory for FPGA configuration.

Backplane Interface

The SCFE-V5-VXS implements a high-speed bi-directional VXS (VITA 41) interface for high-speed data transfer within a switch fabric network, and a RACE++ interface for data communication within currently deployed systems.

The VXS interface offers up to eight lanes (grouped in fours) capable of operating at up to 3.125 Gb/s per lane (maximum theoretical). This interface can use either Aurora[®] or serial RapidIO[®] interconnect as the data layer protocol.

The RACE++ interface consists of two RACE++ ports, each capable of operating at up to 264 MB/s (maximum theoretical). For VME64x backplanes, the VXS P0 connector can be depopulated to ensure physical system compatibility.

Software

Mercury provides driver applications for the SCFE-V5-VXS that are supported by the following operating systems:

- Timesys[®] Linux[®]
- VxWorks[®] 5.5

Environmental

The SCFE-V5-VXS has been designed to meet Mercury VH ruggedization specifications. The board has also been developed under a conduction-cooled envelope for applications that require additional ruggedization characteristics. Consult the factory for availability of conduction-cooled modules.

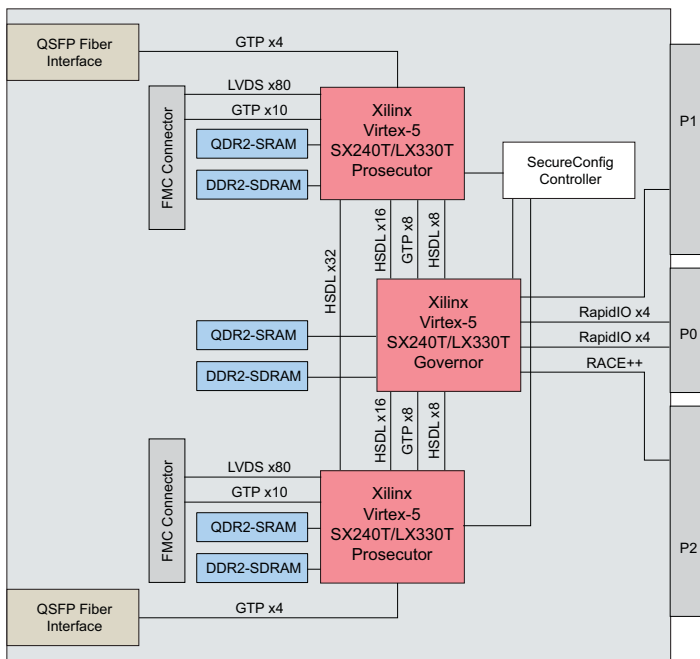


Figure 1. SCFE-V5-VXS block diagram

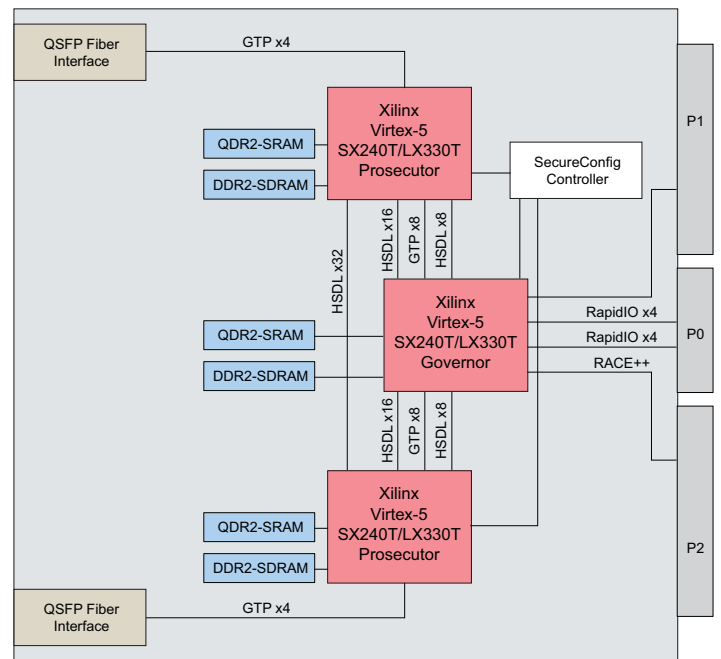


Figure 2. SCFE-V5-VXS block diagram without FMC

Available Options

SCFE-V5-VXS	Standard product
SCFE-V5-FLX-VXS	Standard product with increased I/O capabilities via two VITA 57 FMC sites
SCFE-V5-VME	Standard product without high-speed serial I/O P0 connector
SCFE-V5-FLX-VME	Standard product without high-speed serial I/O P0 connector and with increased I/O capabilities via two VITA 57 FMC sites

Specifications

FPGAs

2 Prosecutors

Xilinx Virtex-5 SX240T or
Xilinx Virtex-5 LX330T

1 Governor

Xilinx Virtex-5 SX240T or
Xilinx Virtex-5 LX330T

Memory

DDR2-SDRAM	3 banks
One bank	256 MB
QDR2-SRAM	3 banks
One bank	9 MB

Datapaths

FMC 1 to Prosecutor 1

80 LVDS pairs at up to 1 Gb/s per pair
10 GTP lanes at up to 3.125 Gb/s per lane

FMC 2 to Prosecutor 2

80 LVDS pairs at up to 1 Gb/s per link
10 GTP lanes at up to 3.125 Gb/s per lane

Prosecutor FPGA 1 to QSFP 1

4 GTP lanes at up to 3.125 Gb/s per lane

Prosecutor FPGA 2 to QSFP 2

4 GTP lanes at up to 3.125 Gb/s per lane

Prosecutor FPGA 1 to Prosecutor FPGA 2

32 full-duplex HSDL links at up to 4 GB/s

Prosecutor FPGA 1 to Governor FPGA

16 full-duplex HSDL links at up to 2 GB/s
8 full-duplex HSDL links at up to 1 GB/s
8 GTP lanes at up to 3.125 Gb/s per lane

Prosecutor FPGA 2 to Governor FPGA

16 full-duplex HSDL links at up to 2 GB/s
8 full-duplex HSDL links at up to 1 GB/s
8 GTP lanes at up to 3.125 Gb/s per lane

Environmental

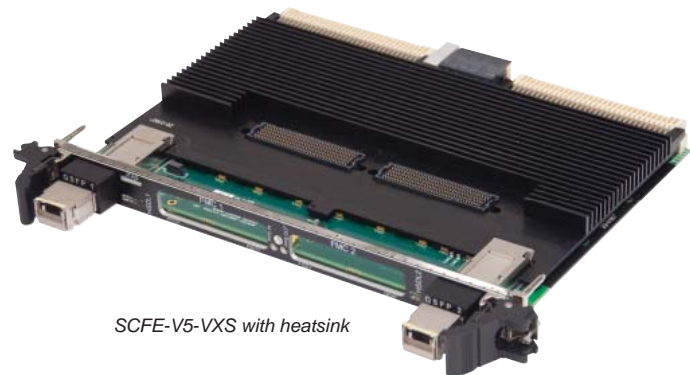
Ruggedization VH

Temperature

Operating 0°C to 40°C with 15 CFM per slot of airflow
Storage -40°C to +85°C

Conduction-cooled

Consult factory.



SCFE-V5-VXS with heatsink

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