

Ensemble 6000 Series OpenVPX HCD6410 Module

High-Density Processing Plus I/O in a Single VPX Slot

- VITA 46/48 (VPX-REDI) 6U serial RapidIO®-enabled module
- Four dual-core MPC8640D processors at 1.06 GHz
- Air-cooled and conduction-cooled models available
- Identical software infrastructure across Mercury products
- Architected to meet OpenVPX™ design principles



The Ensemble™ 6000 Series OpenVPX HCD6410 High Compute Density module from Mercury Computer Systems is designed as a VITA 46 VPX-compliant module in a 6U form factor, also compatible with OpenVPX™ system architecture design principles. This module is a Quad 8640D processing module that combines high-performance Power Architecture™ processing with various I/O capabilities and the scalable serial RapidIO® interconnect. Designed to meet the needs of a variety of applications and deployed environments, the HCD6410 module's eight processor cores can function as a standalone processing center, or as part of an embedded cluster for high-end digital signal processing. With air-cooled and conduction-cooled variants available, the HCD6410 module can be deployed in a variety of environments with confidence. By implementing independent control, data, and management planes, the HCD6410 module supports mapping of system-level architectures onto independent physical interfaces.

The HCD6410 module is supported by the rich set of features available from the MultiCore Plus® software infrastructure, which allows ease of portability while offering an open software-development architecture.

Power Architecture Processor and Subsystem

Each Freescale™ MPC8640D dual-core processor integrates two standard e600 processor cores, two DDR2 memory controllers, 1 MB of L2 cache, and a flexible system-on-chip I/O subsystem. The dual e600 cores that make up the heart of the chip are inherited from the MPC7448 processor, and each retains the high-performance AltiVec™ vector-processing unit. Algorithms optimized for the AltiVec engine port seamlessly to the MPC8640D. Additionally, increased bandwidth among both memory and external I/O and

the processing cores allows efficient processing beyond that available with prior families of Freescale processors. The MPC8640D processor is a pin-compatible enhancement to the MPC8641D that delivers the same performance with a reduced power draw.

The HCD6410 module can be configured with either 1 GB or 2 GB of DDR2 SDRAM per MPC8640D device. Each MPC8640D has its own independent 128-MB write-protectable boot/application flash with protected boot vector to avoid accidental erasure. This flash architecture allows each node to boot independently from other nodes on the module, avoiding contention for a single resource that may impact boot time, and supporting the modular architecture of the HCD6410 module.

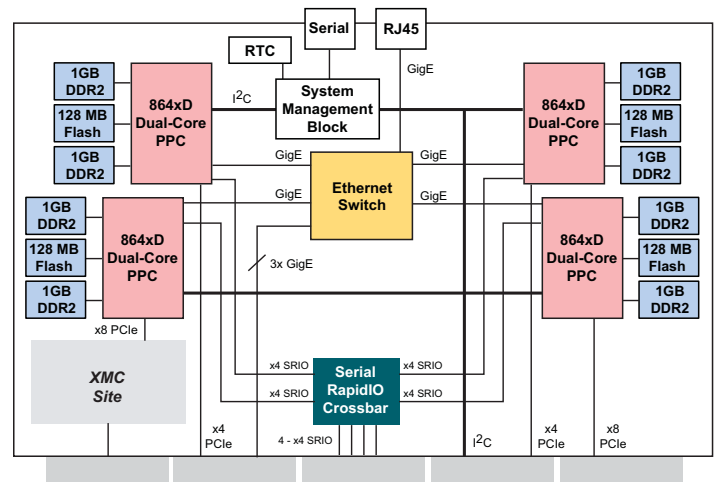


Figure 1. Ensemble 6000 Series OpenVPX HCD6410 Module functional block diagram

Off-Board Connectivity for Data Movement

Per the VITA 46.3 standard, four 4x lanes of serial RapidIO are available for high-bandwidth data movement between processors and off-board. Supporting serial RapidIO data rates at up to 3.125 Gbaud, the on-board RapidIO crossbar links the HCD6410 module to other modules in the system, as well as interconnecting the on-board MPC8640D processors.

The serial RapidIO links can be used to create smaller systems with a RapidIO data plane mesh. For larger architectures, the data plane can be switched by a VPX switch module, such as the Ensemble 6000 Series SFM6100 module. A PCI Express expansion plane complements this serial RapidIO data plane. The PCIe lanes can be used to connect to other VPX modules with PCIe endpoints.

Mezzanine Card Flexibility

The standard XMC site local to the HCD6410 module can be configured with off-the-shelf mezzanine cards using PCI Express protocols. XMCs configured for x8, x4, x2, and x1 PCIe are supported on the J5 connector per the VITA 42.3 standard. XMC user I/O is mapped to the backplane via the J6 connector in accordance with the VITA 46.9 draft standard (x12+8D variant).

Strong Control-Plane Architecture

The HCD6410 module implements a strong control-plane architecture via Gigabit Ethernet. An on-board Ethernet switch is paired with processor and I/O connectivity to drive system-level Ethernet architectures with the HCD6410 module:

- Each HCD6410 module implements an on-board unmanaged Ethernet switch, which links each of the MPC8640D processors to each other.
- On air-cooled variants, a single 1000BASE-TX Gigabit Ethernet connection to the front panel routes to the on-board Ethernet switch. An identical Gigabit Ethernet link is brought to the backplane on both air-cooled and conduction-cooled variants.
- Two 1000BASE-BX Gigabit Ethernet connections are brought to the backplane from the on-board Ethernet switch. These links can connect to additional HCD6410 or HCD6220 modules directly, or be switched by a VPX switch module, such as the Ensemble 6000 Series OpenVPX SFM6100 module.

System-Management Plane

The HCD6410 module follows OpenVPX design principles in leveraging the robust, scalable, and well-tested system-management infrastructure from the AdvancedTCA[®]/MicroTCA[®] architecture. Using the standard I²C bus and IPMI protocol, the on-board system-management block implements the Intelligent Platform Management Controller (IPMC) in accordance with the draft VITA 46.11 standard. This allows the HCD6410 module to:

- Read sensor values
- Read and write sensor thresholds, allowing an application to react to thermal, voltage, or current variations that exceed those thresholds
- Reset the entire module
- Retrieve module FRU (Field Replaceable Unit) information
- Power up/down the entire module
- Be managed remotely by a Chassis Management Controller at the system level, such as that implemented on the Ensemble 6000 Series OpenVPX SFM6100 Switch Module

VPX-REDI

The VPX (VITA 46) standard defines 6U and 3U board formats with a modern high-performance connector set that is capable of supporting today's high-speed fabric interfaces, such as RapidIO. VPX is most attractive when paired with the Ruggedized Enhanced Design Implementation standard – REDI (VITA 48). The HCD6410 module is implemented as a 6U conduction-cooled implementation of VPX-REDI, with air-cooled variants in the same VPX form factor available for less rugged environments.

Targeted primarily for harsh-environment embedded applications, VPX-REDI offers extended mechanical configurations supporting higher functional density, such as two-level maintenance (2LM). 2LM allows relatively unskilled maintenance personnel to replace a failed module and restore the system to an operational state in a limited time period.

Additional Features

The HCD6410 module provides the features typically found on a single-board computer (SBC). In addition to the sophisticated management subsystem and fabric interconnect, the HCD6410 module provides users with a toolkit enabling many different application use cases.

Features include:

- Thermal and voltage sensors integrated on-board
- Real-time clock with granularity to 1 ms and time measurement of up to 30 years
- General-purpose timers/counters per MPC8640D device for synchronization that can interrupt the device upon expiration
- Watchdog timer that can take various actions upon expiration, such as interrupting the processor, resetting the node, or resetting the module
- Open, leveraged, and independent node architecture that supports independent network booting, as well as independent booting from each processor's on-board flash memory
- RS-232 serial ports that are routed to the backplane from each processor, with an additional port routed to the front panel on air-cooled variants
- GPIO lines and several additional bused signals that enhance the system-level functionality of the HCD6410 module

Open Software Environment

Mercury leverages over 25 years of multicomputer software expertise, including recent multicore processor expertise, across its many platforms. This strategy is fully applied to the HCD6410 module. Because the processor, memory, and surrounding technologies are leveraged across product lines, software developed on the HCD6410 module can interface seamlessly with other Mercury products. The same Linux® or VxWorks® development and run-time environment is implemented on the HCD6410 module as on other Mercury systems, such as the Ensemble 7100 HCD7500 module and the Ensemble 5000 Series HCD5220 module.

The MultiCore Plus® (MCP) **MultiCore Plus®** open software environment gives the HCD6410 module access to a wide ecosystem of stacks, middleware, libraries, and tools. The Scientific Algorithm Library (SAL) is optimized for the on-board Altivec™ engine and is available to give the HCD6410 industry-leading signal processing performance. In addition, a key software package available for the HCD6410 module is MultiCore SAL (MCSAL). MCSAL offers the familiar SAL API interface, but is optimized for the multiple on-chip cores available with the MPC8640D.

Software support is available on the HCD6410 module for the following products:

- Open Development Suite for Linux is an Eclipse-based integrated development environment that includes a C/C++ optimizing compiler, a source-level debugger, a language-sensitive text editor, a performance profiler, a project builder, a version control system, a run-time error checker, and a graphical source browser. Mercury provides extensions that allow multi-processor-aware process launch and debug, as well as a System Supervisor view that allows graphical remote management.
- Support is provided for Wind River Workbench integrated development environment when the module is running VxWorks
- Trace Analysis Tool and Library (TATL™) is a “logic analyzer for software” that provides insight into the dynamic interaction of up to a few hundred processors.
- Support for Mercury's standard numeric libraries, VSIPL and SAL (Scientific Algorithm Library), is optimized for the MPC8640D architecture of the HCD6410 module.
- Interprocessor Communication System (ICS) support is carried forward from the RACE++®/MCOE™ software environment. ICS provides a low-level interprocessor communication API that lets users take advantage of the high-bandwidth, low-latency serial RapidIO fabric with an easy-to-use software interface.
- Performance Porting Kit provides low-level handles for manipulation of the serial RapidIO fabric and can be used for simple data movement, or as a base on which to build a custom middleware layer.

The MCP software environment lets applications use industry-standard middleware such as MPI, DRI, CORBA, or standard TCP/IP sockets ported to run seamlessly over the fabric. MCP also offers a software tool that can help to migrate legacy applications created with MCOE into the MCP domain.

Open Standards Means Interoperability and Planning for the Future

The OpenVPX Industry Working Group is an industry initiative launched by defense prime contractors and COTS system developers, to take a proactive approach to solving the interoperability issues associated with the VITA 46 (VPX) family of specifications. This group is actively collaborating to create an overarching System Specification defining VPX system architecture through pinouts definition to establish a limited set of application-specific reference solutions. These OpenVPX™ standard solutions will provide clear design guidance to COTS suppliers and the user community, assuring interoperability across multi-vendor implementations. The OpenVPX™ System Specifications will be introduced into the VSO for ratification to replace the current VITA 46 base and dot specifications in the fall of CY2009.

Specifications

Module

Four dual-core MPC8640D processors
Single XMC site configured for PCI Express per VITA 42.3
Air-cooled or conduction-cooled

Processor Node

Dual-core MPC8640D 1.06 GHz
Cores per device 2
DDR2 SDRAM 1 or 2 GB per MPC8640D device
On-board boot/application flash per MPC8640D device 128 MB

XMC Site

User-defined I/O from P4 to backplane
PCI Express XMC site per VITA 42.3
XMC user-defined I/O from J6 to
backplane via draft VITA 46.9 x8d+x12d standard

Data Plane

Four 4x serial RapidIO links to backplane per VITA 46.3 standard
Co-processor plane for additional data movement via PCI Express

Control Plane

On-board unmanaged Ethernet switch
Front-panel 10/100/1000BASE-TX Ethernet port
(air-cooled variants only)
Backplane 10/100/1000BASE-TX Ethernet port
Two backplane 1000BASE-BX Gigabit Ethernet ports
to on-board Ethernet switch

Management Plane

On-board system management block, including IPMC functionality
Dual IPMI over I²C bus to backplane

Additional Resources

RS-232/RS-422/485 serial interfaces to backplane
Optionally routed to the front panel as RS-232 only on
air-cooled variants
Real-time clock
Watchdog timer
General-purpose 32-bit timers/counters
Thermal, voltage, and current sensors

Environmental

Air-cooled and conduction-cooled variants available.

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