Race SERIES

Mercury Computer Systems, Inc.

FCN Developer's Kit (FDK)

Expert switch fabric, memory, and I/O integration

Open interfaces, shared across products and generations

Faster FPGA development and integration

Mitigates project risks

www.mc.com

The FPGA Compute Node (FCN) Developer's Kit aids customers in developing an FCN application bitstream from a collection of Mercury-supplied reusable IP modules, customer-developed IP modules, and third-party IP modules. The FDK includes Mercury's intellectual property (IP) modules, a validated default bitstream, and an easy-to-use API.

The Mercury Advantage

In the FCN Developer's Kit (FDK), Mercury provides the optimized infrastructure necessary to interface the FPGA application with a high-performance switch fabric, on-board memory, communications, system command and control, and I/O. Typically, vendors delivering an FPGA hardware solution do not provide interfaces for communications, memory, and I/O. They leave development of this critical IP infrastructure for the application designer. Instead of focusing on their application development, FPGA developers first need to tediously build the infrastructure. In contrast, the Mercury-supplied FDK IP modules deliver a prevalidated platform upon which the application designer can build an FPGA application. All Mercury-supplied IP delivers high performance (for example, high utilization of off-chip interconnect bandwidth), while consuming the smallest possible portion of the FPGA's valuable real estate.

Mercury also supplies a sample application and on-board hardware diagnostic testing. To ensure customer success in creating FPGA-based solutions, Mercury includes comprehensive design, consulting, and support services.

Intellectual Property (IP) Modules

Mercury-supplied IP includes the following infrastructure modules:

- RACE-on-Chip (RoC) high-bandwidth interconnect
- Dual-DMA master/slave (DMS) switch fabric endpoint
- Memory controllers for both DRAM and SRAM
- Serial Front Panel Data Port (SFPDP) interface
- Internal control register (ICR) bus
- RoC-to-ICR bridge (RIB)

The Mercury default bitstream (MDB) consists of the Mercury-supplied IP plus a sample application. Customers can study the MDB to gain an understanding of FPGA development, or use it as the framework for their own bitstreams. The MDB is always loaded just prior to the FPGA application and runs the power-on self-test diagnostic software. This means that application bitstreams do not need to have resource-hungry test features incorporated or unique test software developed for them.

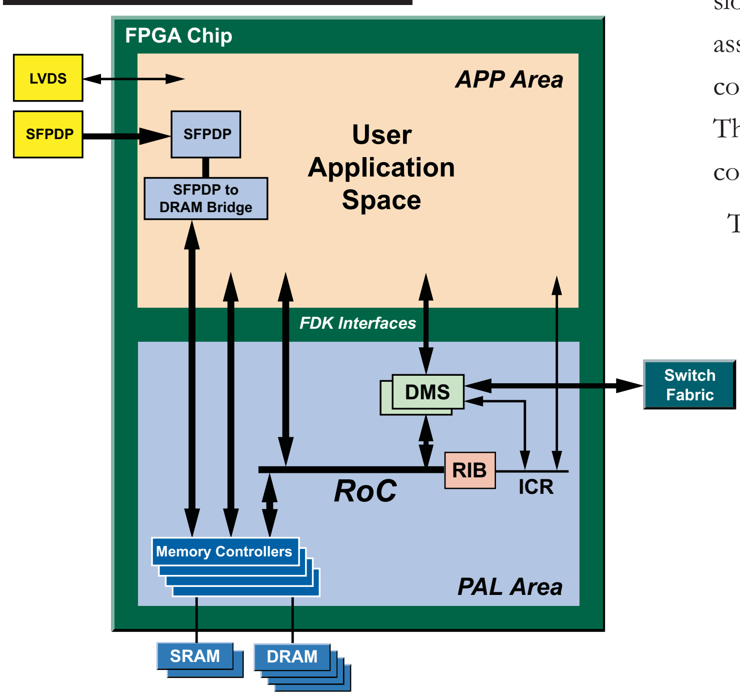
Low-level IP modules, such as memory controllers, are provided by Mercury as relationally placed macros for ultimate performance and reproducible timing closure. VHDL behavioral simulation models of these IP modules are also provided for the best possible simulation performance. Top-level Mercury-supplied IP modules, which stitch together the low-level modules, are transparent and thus modifiable by customers. VHDL sources are provided, so these modules can be successfully used without any changes, or they can be modified or replaced to meet specific design requirements.

RoC Architecture

The RoC (RACE-on-Chip)* bus is the multi-point, high-bandwidth, 64-bit communication pathway for the FCN. The RoC architecture is responsible for the FCN's dramatic high-speed data movement and seamless integration into the multicomputer switch fabric. It is used to extend the multicomputer's memory map into the FCN, allowing any connected module within the FPGA to be visible to the rest of the multicomputer via Mercury's shared memory buffer (SMB) and DMA transfer (DX) APIs.

The RoC bus is implemented in a ring configuration with connected modules participating in a master/slave hierarchy. The FDK provides three types of RoC devices: the dual-DMA master/slave (DMS) endpoint, memory controllers, and the RoC-to-ICR bridge (RIB). Through a public interface, the user application can also have a high-bandwidth, burst-transfer RoC connection. The FDK architecture diagram in Figure 1 shows the RoC bus and all its associated modules.

Figure 1 FDK IP Module Architecture



* Patent Pending

The DMS modules are the backbone of FCN data movement, connecting the FCN to the switch fabric and acting as either a master or slave on the RACE++® switch fabric. Presently, a DMS module is always a master on the RoC bus. An FCN can support up to two DMS devices with each DMS connected to a separate switch fabric endpoint. Each DMS contains a 2-channel DMA engine. The user FPGA application can directly connect to the DMS endpoint for initiation of DMA transfers and flow control. See Figure 1, FDK IP Module Architecture.

The internal control register (ICR) bus is the lightweight command and control communication pathway for the FCN. For example, the ICR bus can be used to write parameters to IP modules and to read FDK module status. The ICR bus is physically eight bits wide for minimal FPGA resource usage, and logically 32 bits wide for ease of software programming.

The RIB is a slave on the RoC bus and the master on the ICR bus. Other devices on RoC or the multicomputer switch fabric can initiate data transfer to (or "indirectly master") the ICR through the RIB. The RIB supports transfer widths of 32 and 64 bits and provides any necessary endian conversions between the RoC bus and the ICR bus. Registers assigned to the ICR bus are mapped into the Mercury multicomputer address space, making them globally accessible. The ICR bus provides 16 MB of memory for mapping control registers. See Figure 1.

The memory controllers connect to SRAM chips and DRAM chips external to the FPGA, and to the RoC bus and the user application within the FCN. This is accomplished with three interfaces on each memory controller:

- The interface to the RoC bus makes the memory visible to devices on RoC and the multicomputer switch fabric.
- The user interface connects to application logic.
- The external interface can be used by the application developer to connect to I/O modules.

The memory controllers are optimized for burst transfers to increase system performance. The SRAM memory controllers also include a fast random access capability.

Input/Output

In addition to full switch fabric connectivity, the FDK gives the FCN application a connection to various types of I/O directly attached to the FPGA. Both off-module and FPGA-to-FPGA "meshing" connections are provided. Depending on the board type being targeted, both parallel LVDS and high-speed serial I/O may be available. See Figure 1.

Inside the FPGA, the I/O is part of the application area. I/O can be routed in one of three ways:

- Connected directly to its processing logic or custom protocol
- Connected to a memory controller
- Bridged to the RoC or ICR bus

For FCNs that have RocketIO™ high-speed serializer/deserializers, including those found on the MCJ6 FCN board, the FDK provides a serial front panel data port (SFPDP) IP module. IP modules for other high-speed serial protocols are provided by third parties or may be developed by the user.

Low-voltage differential signaling (LVDS) parallel I/O connections provide the ultimate in flexibility. The FPGA application developer can specify the I/O direction, driver type, clocking, and termination of each individual pin. See Figure 1.

Bitstream Build and Simulation Tools

The FDK provides a hardware description language (HDL)-based environment using VHDL. VHDL was chosen for its powerful abstraction capabilities; however, using mixed language versions, Verilog can also be used by the FPGA application developer. It is also possible for the user to work with higher level tools, by adapting them to the well-specified HDL interfaces provided in the FDK.

Table 1 Third-Party Tools

Tool Type	Tool Name	Vendor
Simulation	ModelSim™	Mentor Graphics
Synthesis	Synplify®	Synplicity
Place and Route	ISE™	Xilinx
Memory Simulation	MMAV™	Denali

Mercury FCN products are built for easy integration with leading third-party FPGA development tools. The leading toolsets, shown in Table 1, are currently certified for use with Mercury FCN systems. Mercury certifies that, if the supplied IP is not altered and the recommended third-party tools and versions are used, customers can build an exact duplicate of the supplied MDB. Use of alternate third-party tools or versions may have unpredictable results.

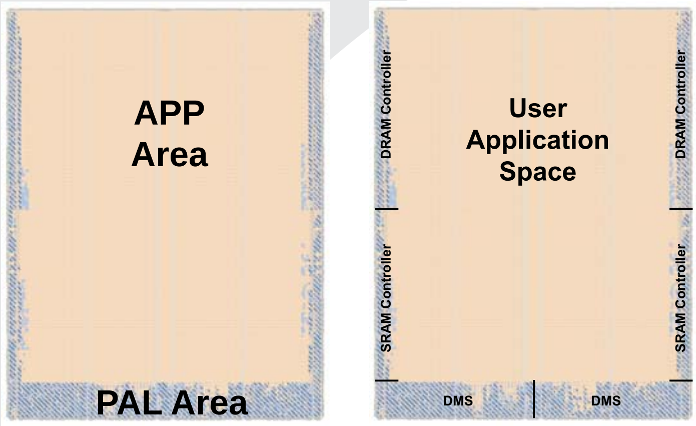
These tools are not supplied by Mercury and should be obtained directly from the tool vendors. Contact your Mercury sales representative for specific recommended tool versions. Other tools can be evaluated in response to customer requests.

Simulation and Debug

For simulation, the FDK includes a test harness that models a complete FPGA compute node, not just the FPGA. This harness includes bus functional models (BFMs) for each of the interfaces to the FPGA in the FCN. The BFM for the RACE++ switch fabric includes the ability to do programmed I/O, burst, and DMA transfers. The RACE++ BFM also models memory on the switch fabric that may be a data source or destination for DMA being done by the FPGA. For the memory controllers, models of the memory chips are provided, and there is an option to use third-party Denali memory models. Users can insert their own model for parallel LVDS I/O to match their own custom I/O. For high-speed serial I/O, the FDK includes a BFM for SFPDP.

Developers prefer to debug in simulation, where possible, due to enhanced controllability and visibility. However, debugging on the real hardware is often necessary. The Supervisor tool from Mercury provides status and monitoring of the FPGA, in a real system, including temperature and current consumption. The ChipScope™ tool from Xilinx® can be used to embed a logic analyzer into the FPGA application. The parallel LVDS I/O can be connected to an external piece of test equipment such as a logic analyzer. The ICR bus can be used within the FPGA application to read and control user-defined debugging logic in the FPGA. RoC provides access to all connected memories, so that their contents can be dumped or loaded from the switch fabric.

Figure 2 FPGA Floor Plan



Pulling It All Together

The FDK supplies two abstract containers to simplify design: the platform abstraction layer (PAL) and the user application (APP) area. The PAL contains the Mercury-supplied infrastructure IP previously discussed, and provides the developer with high-level interfaces to other FCN components. The APP area contains the user application IP. The FPGA floor plan, in Figure 2, shows the location and approximate size of the APP and PAL areas and associated IP modules in a Xilinx 3-million gate (Virtex II™ 3000) part, Mercury's smallest FCN. These diagrams clearly show that the FDK design uses minimal FPGA real estate for PAL infrastructure, leaving the majority of the FPGA resources for the application.

Figure 3 Typical FCN-Based Board

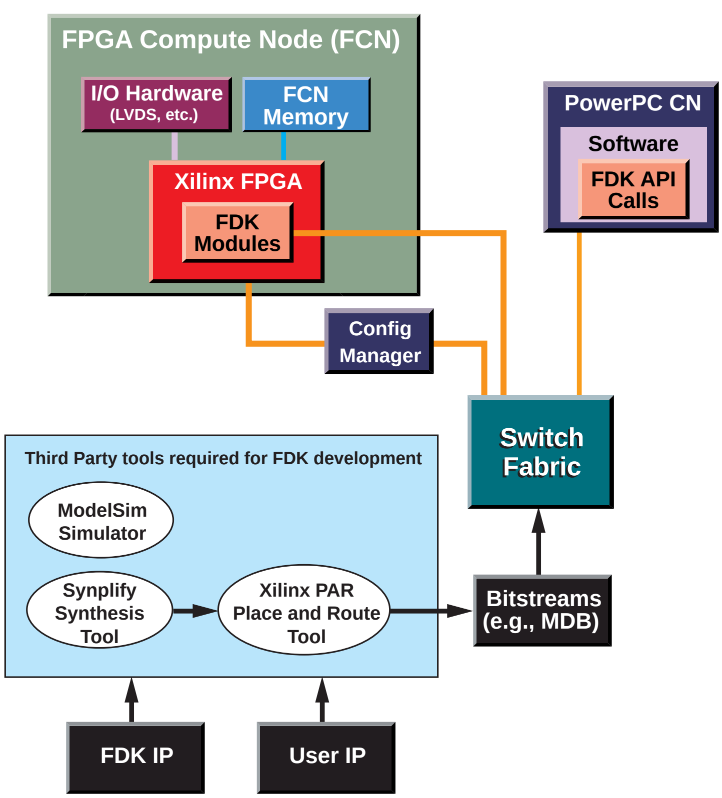


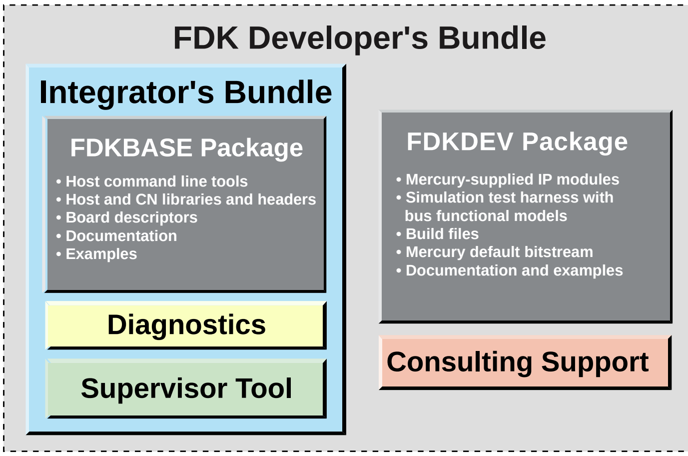
Figure 3 shows a block diagram of a typical FCN-based board, which can have one or more FCNs and zero or more PowerPC® CNs. The FCNs are fully integrated switch fabric endpoints. FPGA bitstreams are created off-line on a development platform using third-party tools, not supplied by Mercury. The final bitstreams are loaded to the FPGA via switch fabric connections. Because Mercury hardware supports the theoretical maximum rate of FPGA loading, FPGA reconfigurations (bitstream reloads) can be accomplished in less than 100 msec.

FDK Packaging

The FCN Developer's Kit contains five principal components: the FDKBASE package, hardware diagnostic software, the Supervisor tool, the FDKDEV package, and engineering consulting support. As shown in Figure 4, the FDK is available in two bundles designed for different customer requirements. Your Mercury sales representative can help you select the best bundle for your FPGA program needs.

- The Integrator's Bundle is for system developers who are not developing VHDL code, but are integrating the FCN into a multicomputer application. The Integrator's Bundle would be most useful for those developers who need a turnkey "black box" FPGA solution and who are tasked with integrating it into the Mercury multicomputer system.
- The Developer's Bundle is for developers actually creating FPGA application IP modules in VHDL. It contains all the Mercury-supplied IP and software necessary for development of FPGA applications. The Developer's Bundle includes one seat of the Integrator's Bundle and a design services agreement. See Figure 4.

Figure 4 FDK Packaging Options



Consulting Support

Mercury's strategy for simplifying the FPGA development project includes providing initial service offerings as an integral part of each initial FDK Developer's Bundle license.

As part of this program, each initial FDK Developer's Bundle customer receives an engineering consulting support agreement, which includes two design reviews and 20 hours of design support services. Note that additional FDK Developer's Bundle seats do not include additional service agreements, which are available for an additional fee. This service helps mitigate project risks and reduce FPGA application development startup time.

Training

Once developers complete third-party tool training, they can take a Mercury FPGA development course designed to train them in FCN application development and integration into the Mercury multiprocessing system.

System Requirements

	VantageRT® FCN-based System*s	MCJ6 FCN-based Systems
Mercury Product Line	VantageRT PCI	6U VME
Operating Environment	MCOE 6.2.0 or higher	
FDKDEV Development Host OS	Windows® XP Professional	
FDKBASE Development Host OS	Windows XP Professional	Solaris™ 8
Runtime Host OS	Windows XP Professional	VxWorks®
FDKDEV Development Host Hardware	Pentium® III and later	
FDKBASE Development Host Hardware	Pentium III and later	UltraSPARC®
Runtime Host Hardware	Pentium III and later	MVME 5110

* See VantageRT FCN data sheet for power and cooling requirements.

For more information, go to www.mc.com

RACE-on-Chip (RoC) technology is patent pending.

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Mercury Computer Systems, Inc.

The Ultimate Performance Machine

199 Riverneck Road
Chelmsford, MA 01824-2820 U.S.A.
978-256-1300 • Fax 978-256-3599
800-229-2006 • http://www.mc.com
NASDAQ: MRCY

Nihon Mercury Computer Systems K.K.
No. 2 Gotanda Fujikoshi Bldg. 4F
5-23-1 Higashi Gotanda
Shinagawa-ku, Tokyo 141-0022
JAPAN
+81 3 3473 0140
Fax +81 3 3473 0141

Mercury Computer Systems, SARL
Immeuble le Montreal
19 bis, avenue du Quebec
Villebon
91951 COURTABOEUF CEDEX
FRANCE
+ 33 (0) 1 69 59 94 00
Fax + 33 (0) 69 86 10 87

Mercury Computer Systems, Ltd.
Campbell Court, Unit 19
Bramley, Tadley
HANTS RG26 5EG
UNITED KINGDOM
+ 44 1 256 880090
Fax + 44 1 25688 4004