

# ECV4-2 Two/Four-Channel, FPGA-Based PMC/XMC Digital Receivers

High-Speed A/D Conversion, Resolution from 8 Bits to 16 Bits

- Processing power from two Virtex™-4 FPGAs
- Optimized for wideband multi-channel data processing
- Multiple configurations for multiple missions
- Air-cooled or conduction-cooled



ECV4-2-2R105

The Echotek™ Series ECV4-2 family of wideband digital receivers from Mercury Computer Systems implements a flexible field-programmable gate array (FPGA) based architecture in a space-efficient PMC/XMC form factor. The flexibility and power of the Virtex™-4 FPGAs allow the family to deliver unique capabilities, such as multi-board coherency, while addressing a range of analog signal requirements.

### Analog Flexibility

Each member of the ECV4-2 family provides unique I/O connectivity and functionality. Each card is configured with a specific set of A/D and/or D/A converters addressing a defined bandwidth and frequency for data conversion. Cards are available in two- and four-channel versions, with A/D, D/A, and transceiver configurations. The cards also include various clocking and synchronization inputs and outputs.

### Unique Application Suitability

The ECV4-2 family is designed to support a broad range of digital receiver applications. The receiver channel synchronization allows all important receiver functions to be synchronized across all receiver channels in a multi-board configuration using front-panel sync input and sync output connectors. This capability makes the ECV4-2 especially well-suited for beamforming and direction-finding as required by radar, SIGINT, ELINT, medical imaging, and communications.

### Processing Power from Two FPGAs

The ECV4-2 product family supports two FPGAs. One Xilinx® Virtex-4 FX, SX, or LX FPGA functions as the primary data processor. This FPGA allows the user to run custom algorithms such as digital down/up conversion (wideband or narrow-band), fast Fourier transforms (FFT), and filtering directly on the board. In support of the FPGA processing power, the board also includes up to 512 MB of DDR SDRAM and 2 MB of dual-port SRAM. The second FPGA is a Virtex-4 LX25, which is dedicated to the PCI/PCI-X interface.

### PCI or PCI-X Connectivity

The second FPGA, a Virtex-4 LX, functions as the board controller and also manages a fully compliant PCI or PCI-X interface. The ECV4-2 family uses the PCI or PCI-X interface for command and control, as well as DMA operations.

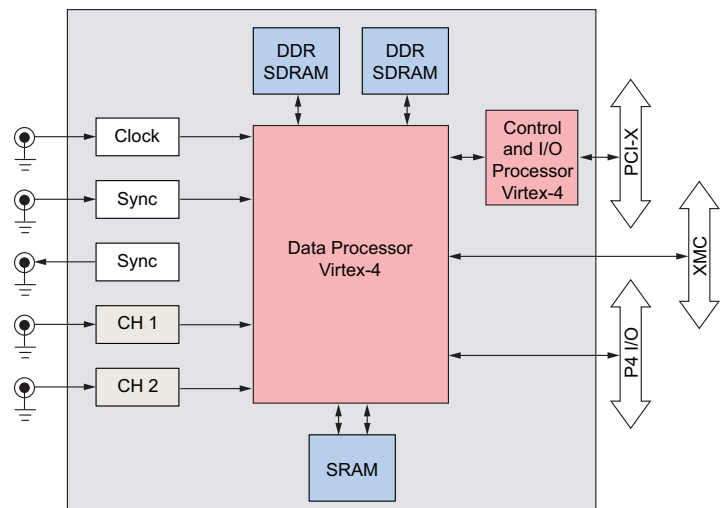


Figure 1. ECV4-2 two-channel component block diagram

## FPGA Development IP

The ECV4-2 is shipped with pre-loaded FPGA IP for the data processor FPGA and the control/IO processor FPGA. The IP is stored in onboard flash memory and loaded into the FPGAs on power-up. Depending on the custom configuration and application of the product, the pre-loaded IP ranges from default board verification IP to custom application IP.

The default board verification IP is typically shipped to customers planning to implement their own IP and includes the basic functionality required to verify the operation of the hardware. Included in this IP package is a PCI/PCI-X interface with AutoDMA capability, as well as various Mercury designed cores. This IP package includes a local control bus (LCB) interface, a DDR SDRAM interface, a dual-port SRAM interface, a high-speed data link (HSDL) interface for inter-FPGA data flow, plus A/D and D/A interfaces with collection control logic. Sophisticated off-chip interfaces such as DDR and source-synchronous LVDS are also included.

Customers developing their own application IP can gain access to this functionality via a simple local user interface. This allows the end-user to focus on developing application-specific functionality and simplifies the integration of that IP.

Users can develop their unique application IP using standard FPGA development tools such as the Xilinx ISE. The end-user can easily integrate the IP into the board by downloading the end-user images into the field-upgradeable flash memory over a simple memory map PCI/PCI-X interface.

## Flash Memory to Program FPGAs

The ECV4-2 supports up to 16 MB of flash memory that is used to program both FPGAs, which can be reconfigured from the flash at any time. The flash itself can also be reprogrammed at any time.

## Air-Cooled or Conduction-Cooled

Select members of the ECV4-2 product family are available in air-cooled or conduction-cooled versions. Conduction-cooled versions comply with the VITA 20-2001 standard.

## Software Support

Mercury provides driver applications for the ECV4-2 supported by the following operating systems:

- Linux®
- VxWorks®

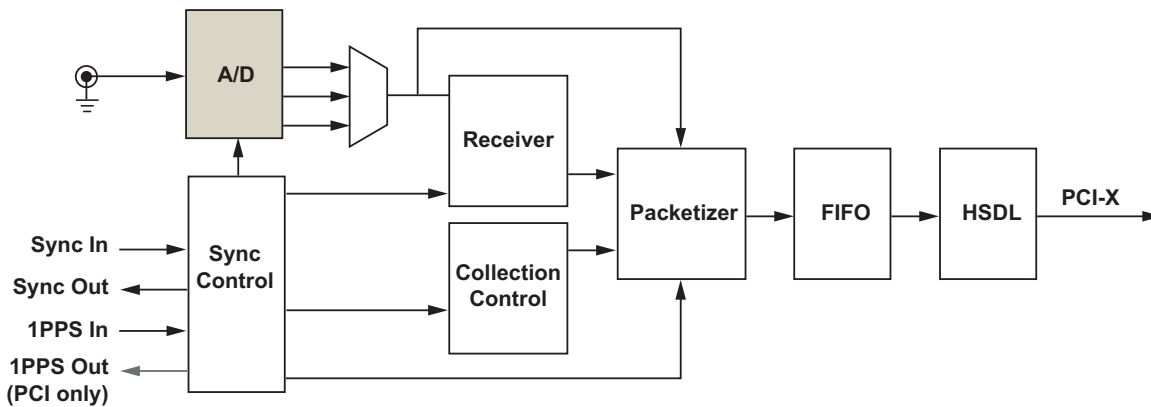


Figure 2. ECV4-2 functional block diagram

## Options to Fit a Range of Applications

The ECV4-2 family offers a range of options to address a broad variety of application requirements. The models are described in the following table.

ECV4-2 Models

Product	Data Conversion	Clock Capabilities	Memory Structure	Sync Structure
ECV4-2-2R105-PMCX/XMC	2-channel, 14-bit, 105-MHz A/D (AD6645)	1 external reference clock input, 30 MHz – 105 MHz (SSMC)	2 – 128-MB banks DDR SDRAM (Option: 256-MB banks) 1 – 512K x 36 dual-port SRAM	2 sync inputs (SSMC) 1 sync output (SSMC)
ECV4-2-2R1500-PMCX/XMC	2-channel, 8-bit, 1.5-GHz A/D (ADC08D1520)	1 external reference clock input, 600 MHz – 1.5 GHz (SSMC)	2 – 128-MB banks DDR SDRAM (Option: 256-MB banks) 1 – 512K x 36 dual-port SRAM	2 sync inputs (SSMC) 1 sync output (SSMC)
ECV4-2-2R130-1T500-PMCX/XMC	2-channel, 16-bit, 130-MHz A/D (LTC2208) 1-channel, 16-bit, 500-MHz D/A (DAC 5686)	1 external reference clock input, 1 MHz – 320 MHz (SSMC)	2 – 128-MB banks DDR SDRAM (Option: 256-MB banks) No dual-port SRAM	2 sync inputs (SSMC) 1 sync output (SSMC)
ECV4-2-4R130-PMCX/XMC	4-channel, 16-bit, 130-MHz A/D (LTC2208)	1 external reference clock input, 1 MHz – 130 MHz (SSMC)	2 – 128-MB banks DDR SDRAM (Option: 256-MB banks) No dual-port SRAM	1 sync input (SSMC) 1 sync output (SSMC)
ECV4-2-2R130-2T500-PMCX/XMC	2-channel, 16-bit, 130-MHz A/D (LTC2208) 2-channel, 16-bit, 500-MHz D/A (DAC 5686)	1 external reference clock input, 1 MHz – 320 MHz (SSMC)	2 – 128-MB banks DDR SDRAM (Option: 256-MB banks) No dual-port SRAM	1 sync input (SSMC) 1 sync output (SSMC)
ECV4-2-2R130-2T500-PCIX	2-channel, 16-bit, 130-MHz A/D (LTC2208) 2-channel, 16-bit, 500-MHz D/A (DAC 5686)	1 external reference clock input, 1 MHz – 320 MHz (SSMC)	2 – 128-MB banks DDR SDRAM (Option: 256-MB banks) No dual-port SRAM	2 sync inputs (SSMC) 1 sync output (SSMC)
ECV4-2-2R130-SL-PMCX	2-channel, 16-bit, 130-MHz A/D (LTC2208)	1 external reference clock input, 33 MHz – 130 MHz (SSMC)	2 – 128-MB banks DDR SDRAM (Option: 256-MB banks) 2-MB DDR2 SRAM	2 sync inputs (SSMC) 1 sync output (SSMC)

## Specifications

### FPGAs

2 FPGAs total      208 XtremeDSP slices  
8,064 KB of block RAM  
119,088 logic cells

Note: FPGA specifications may vary, based on FPGA model selection.

1 data processor      Xilinx Virtex-4 XC4VFX60 or XC4VFX100

1 control processor      Xilinx Virtex-4 XC4VLX25

### Memory

#### DDR SDRAM

256 MB with two banks of 2 x 32M x 16-bit chips or  
512 MB with two banks of 2 x 64M x 32-bit chips

Dual-port SRAM\*      2 MB 512 KB x 36-bit chips

\*SRAM is available only on certain models.

### Data Paths

SRAM to data processor  
Dual-port, 400 MB/s per port, 800 MB/s aggregate

DDR SDRAM to data processor  
Two banks, 1.328 GB/s per bank, 2.656 GB/s aggregate

Data processor to control processor  
Two 800 MB/s parallel LVDS buses  
Each configurable in both directions

Data processor P4 I/O interface  
Available LVDS pairs differ by board model

PCI/PCI-X support  
133 MHz or 100 MHz 64-bit PCI-X supported, 33 MHz 32-bit PCI also supported – all PCI/PCI-X signaling is 3.3 V

## Environmental Specifications

The ECV4-2 family offers multiple ruggedization levels. Select family members are offered with conduction-cooling.

Ruggedization Level	Commercial	Conduction Cooled*
Temperature		
Operating	0°C to 40°C with 300 ft/s appropriate airflow	-40°C to +70°C at the normal interface
Storage	-40°C to +85°C	-20°C to +80°C
Humidity	Up to 95% RH	Up to 95% RH with varying temperature, 10 cycles, 240 hr
Cooling	Cooled by blown air, for use in benign environments and software development applications.	Mechanically compliant with IEEE-1101.2-1992. Designed for severe environment applications with high levels of shock and vibration, small space envelope, and restricted cooling. Optional environment stress screening.

\*Available only on certain models. Check with your Mercury sales representative for product availability.

This product is subject to the controls of the Export Administration Regulations (EAR). This product shall not be provided to non-U.S. persons or transferred by any means to any location outside the United States without approval from the U.S. Department of Commerce.

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