

Dual Cell-Based Blade 2

Single-Slot Blade Solution Based on the Cell BE Processor

- Outstanding performance density for high-performance computing applications
- Generous I/O bandwidth and memory
- Optional Cell-optimized software for enhanced application performance and developer productivity
- Designed for IBM BladeCenter® H chassis
- Processing density exceeds 1 TFLOPS per cubic foot



The Dual Cell-Based Blade 2 (DCBB2) from Mercury Computer Systems is a second-generation product based on the Cell Broadband Engine™ (BE) processor and the open IBM BladeCenter® standard for managed server chassis. Fourteen single-slot DCBB2 units fit in a 9U BladeCenter H chassis, providing a processing density of greater than 1 TFLOPS per cubic foot.

The DCBB2 solution offers Mercury customers the advantages of the Cell BE processor in a package designed for high-performance environments. The DCBB2 significantly improves performance for graphic-intensive workloads and computationally intensive high-performance computing (HPC) applications in medical imaging, industrial inspection, aerospace and defense, seismic processing, telecommunications, and other industries. Performance scales dramatically when the application is distributed across multiple blades in a cluster or across the network.

Superb Performance

The DCBB2 has two Cell BE processors. Each processor running at 3.2 GHz has 205 single-precision GFLOPS of performance in the SPE (synergistic processing element) array, for a total of 410 GFLOPS on the blade. Mercury has mapped key signal processing algorithms onto the blade, significantly increasing the performance advantages for high-performance computing applications, whether measured in performance-per-Watt or performance-per-dollar.

Multicomputer-on-a-Chip

The Cell BE processor architecture is essentially a multicomputer-on-a-chip. This architecture of heterogeneous high-performance processing elements on a common interconnect has a structure that is designed for distributed processing.

The Cell BE processor includes three main functional components:

- The Power™ processing element (PPE) has dual hardware multi-threading and a standard VMX vector processing engine. It has separate 32 KB L1 data and instruction caches and 512 KB of L2 cache.
- In the array of eight SPEs, each has a dual-issue pipeline, a 128-bit-wide vector processing engine, a large register set (128 registers, each 128 bits wide), and 256 KB of local store (LS). Each SPU accesses system memory via its memory flow controller (MFC), which is a high-performance DMA engine.
- A high-speed data ring called the element interconnect bus (EIB) consists of two pairs of counter-rotating rings with a sustained aggregate bandwidth of 205 GB/s.

Additionally, each chip has high-bandwidth, low-latency memory and I/O interfaces.

The DCBB2 has two Cell BE processors operating in SMP mode with full cache and memory coherency. The EIB is extended transparently across a high-speed coherent interface running at 20 GB/s in each direction between the two Cell BE processors.

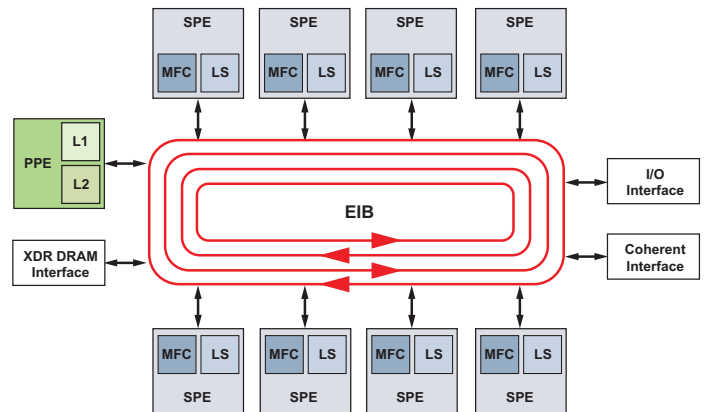


Figure 1. Cell Broadband Engine Processor block diagram

Dual Cell-Based Blade 2 Topology

The DCBB2 has two Cell BE processors directly mounted on the board, providing multiprocessing capabilities. The blade can include an optional serial attached SCSI (SAS) disk controller that can connect to redundant BladeCenter SAS switches via the midplane. The blade's front panel provides local power control, soft reset, removable storage control, and LEDs for power, alert, and status information. The serial interface to each blade is accessible via the rear of the BladeCenter H chassis.

Companion Chips

Each Cell BE processor has a companion chip that adds rich functionality and high performance to complement the processor. Each companion chip incorporates a high-performance, multi-channel DMA engine with striding and list DMA support. It also includes a low-latency mailbox mechanism for intra-blade event notification between Cell processors.

The two companion chips also provide the memory and I/O features detailed in the following sections.

High-Speed Memory

The XDR™ DRAM device architecture allows the highest sustained bandwidth for multiple, interleaved randomly addressed memory transactions. The DCBB2 includes 1 GB of XDR DRAM per Cell BE processor.

In addition, two DDR2 DIMM sockets are attached to each companion chip supporting up to 1-GB DIMMs each. In total, the DCBB2 can support up to 10 GB of memory.

PCI Express® Interface

PCI Express is a high-speed serial interface with a packet-based protocol. Each Companion Chip implements 24 lanes of PCI Express; the total sustained theoretical bandwidth to the blade is almost 10 GB/s simultaneously in each direction. The DCBB2 provides two PCI Express x8 interfaces connecting to a high-speed daughtercard site that can accept cards such as the InfiniBand® 4X HCA expansion card, which provides dual 4X InfiniBand to the midplane.

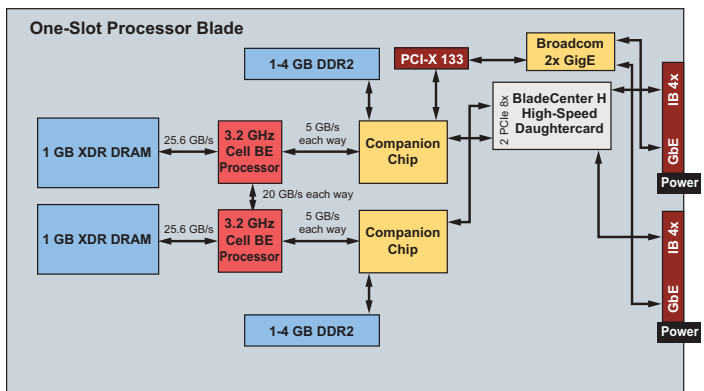


Figure 2. DCBB2 functional block diagram

Gigabit Ethernet

A dedicated Gigabit Ethernet controller chip is connected to the dual Gigabit Ethernet ports on the BladeCenter midplane. The midplane connects to the Gigabit Ethernet switches in the chassis.

MultiCore Plus SDK (Optional)

The MultiCore Plus™ SDK (Software Development Kit) is a suite of software products specifically designed for next-generation multicore processors such as the Cell BE processor. The SDK includes a comprehensive programming framework, highly optimized math libraries, and plugins that integrate the MultiCore Plus software with the IBM IDE, based on the Eclipse IDE.

MultiCore Plus™

The focus of the MultiCore Plus SDK is application performance and developer productivity. This seamless package of software development tools and libraries helps you take full advantage of the Cell BE processor's architecture to maximize your application's resources and boost performance.

The Ready for IBM Technology Mark certifies that the MultiCore Plus SDK has met IBM-specified standards for compatibility with IBM Microelectronics products and services. Ready for IBM Technology solutions are designed to help original equipment manufacturer (OEM) customers speed time to market, reduce development risk, lower development costs, and improve return on investment.



Serviceability Features

Serviceability features include hardware verification during module initialization, light-path diagnostics, an onboard systems-management processor, and a chassis management module. Optional Linux®-based diagnostics verify the correct operation of the blade.

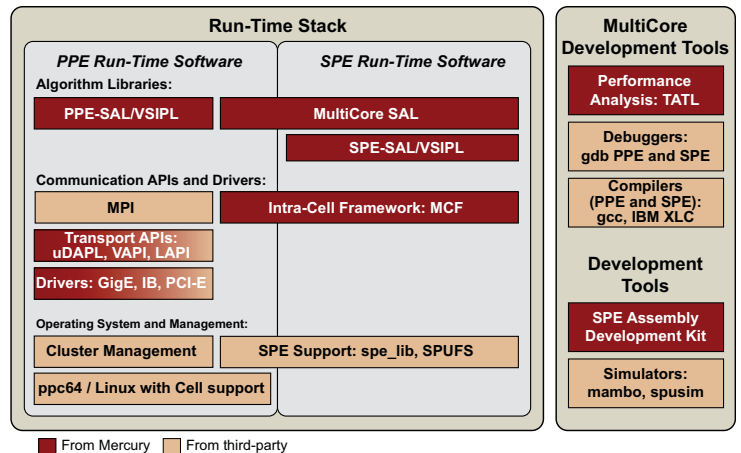


Figure 3. MultiCore Plus SDK software stack

Mercury Support Services

Mercury's enhanced support services augment your internal capabilities and increase your effectiveness. For example:

- Installation and upgrade services span the entire installation process from site planning through onsite installation and certification to post-installation upgrade configuration and testing.
- End-to-end network integration services start with a requirements assessment, include network integration design tailored to your environment, and culminate with the installation and configuration of your total system.
- Flexible product training offerings include one-on-one or classroom setup in small or large groups, with either instructor-led or learn-on-demand format for introductory or advanced classes, refresher training, or certification.
- The self-service maintenance program trains and certifies you to use quick-fix scripts and easy-to-follow instructions, diagrams, and videos to help you perform your own maintenance with spares kits for fast repair and customer-replaceable units.
- On-going maintenance and repair services include remote and onsite support packages tailored to your business needs, standard and extended technical support coverage, and guaranteed response times and parts replacement.

Specifications

Dual Cell BE Processors

PPE core	IBM® 64-bit Power Architecture™
L1 cache size	32 KB instruction; 32 KB data
L2 cache size	512 KB
SPEs	8
Local store	256 KB
Registers	128 x 128 bits wide
EIB	205 GB/s sustained aggregate bandwidth
Processor internal clock speed	3.2 GHz
Processor-to-XDR-memory bandwidth	25.6 GB/s
Processor-to-processor coherent interface	20 GB/s in each direction

Memory

XDR memory (each processor)	1 GB 3.2-GHz XDR DRAM, 2 channels per processor
DDR2 memory (each processor)	1 or 2 GB 667-MHz DDR2 organized as 2 VLP DIMMs per processor, 1 channel per DIMM
ECC support	Single-bit correct; double-bit detect on XDR and DDR2
Flash	32 MB
NVRAM	1 MB

Storage

Optional Serial Attached SCSI controller	300 MB/s
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I/O Subsystems

Dual Gigabit Ethernet port connected to the midplane	
Serial port	Via midplane to rear of chassis
Serial over LAN	Via BladeCenter Advanced Management Module

Expansion Option

High-speed daughtercard

InfiniBand 4X HCA Expansion Card

Additional expansion options are being qualified. Contact your Mercury sales representative for details.

System Management

System management processor	
Baseboard management controller	

MultiCore Plus™ SDK Software (Optional)

(32/64-bit application support)

MCF (MultiCore Framework)	PPE/SPE
TATL™ (Trace Analysis Tool and Library)	PPE/SPE
SAL (Scientific Algorithm Library)	PPE/SPE
PixL™ (Image Processing Algorithm Library)	PPE
MCPDIAG (MultiCore Plus Diagnostics)	PPE/SPE
SPEAD-K (SPE Assembly Development Kit)	SPE
Linux operating system	

Size

Length	446 mm (17.6 in)
Width	245 mm (9.7 in)
Height	29 mm (1.14 in)

The DCBB2 is a single-width blade server in a BladeCenter H 9U chassis.

Environmental

Ambient temperature	5°C to 35°C
Humidity	5-95% non-condensing
Altitude	3000 ft at 35°C 7000 ft at 32°C

Power

Total power	380W
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Conforms to BladeCenter Open Specifications

Compliance

European Directive 2002/95/EC (RoHS 5/6 Server Exemption Directive)	
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